Gain Enhanced On-Chip Folded Dipole Antenna Utilizing Artificial Magnetic Conductor at 94 GHz

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Abstract—On-chip antennas suffer from low gain values and distorted radiation patterns due to the lossy and high permittivity Si substrate. An ideal solution would be to isolate the lossy Si substrate from the antenna through a Perfect Electric Conductor (PEC) ground plane, however the typical CMOS stack up which has multiple metal layers embedded in a thin oxide layer does not permit this. In this work, an Artificial Magnetic Conductor (AMC) reflecting surface has been utilized to isolate the Si substrate from the antenna. Contrary to the previous reports, the AMC structure is completely embedded in the thin oxide layer with the ground plane above the Si substrate. In this approach, the AMC surface acts for the first time as both a reflector and a silicon shield. As a result the antenna radiation pattern is not distorted and its gain is improved by 8 dB. The fabricated prototype demonstrates good impedance and radiation characteristics.

Index Terms—AMC, mm-wave, SoC and, on-chip antenna.

I. INTRODUCTION

MILLIMETER wave frequency bands have recently gained a lot of interest in the field of wireless communications. The multi-GHz of bandwidth available at these bands is suitable for applications that require high data rates or high resolution imaging [1]–[3]. Moreover, the progress made in the silicon (Si) based fabrication processes such as Complementary Mixed Oxide Semiconductor (CMOS) made it possible to realize devices that can operate at the mm-wave frequencies. Although Si-based ICs provide ultimate wireless system integration, especially at mm-wave frequencies, one of its drawbacks is that it is not suitable for antennas implementation [4], [5]. Antennas designed on Si have negative gain values and distorted radiation pattern which can result in interference with other circuitry.

Several methods have been studied in previous reports to overcome the drawbacks of on-chip antennas, especially their low gain values [6], [7]. However, these approaches either complicate the fabrication process, hence increasing the fabrication cost, or add an off-chip component that affects the overall system integration. Since typical CMOS fabrication processes include six to nine metal layers embedded in silicon oxide, one of the metal layers can be considered as a Perfect Electric Conductor (PEC) ground plane to isolate the antenna from the Si substrate. Although this idea caters for the disadvantages of the other approaches, it limits the antenna substrate to the ultra-thin silicon oxide layer, which deteriorates the antenna performance due to its proximity to the PEC ground plane.

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Fig. 1: AMC ground plane locations: (a) previously reported and (b) proposed in this work.

Another approach to shield the antenna from Si without the need of any off-chip components or complicating the fabrication process is the use of Artificial Magnetic Conductors (AMC). A planar AMC is composed of 2D periodically patterned metallic surface, also known as Frequency Selective Surface (FSS) or Partial Reflective Surface (PRS), placed on top of a grounded substrate [8]. AMCs are superior to conventional PEC ground planes, since induced image currents are in-phase and they can be designed to have zero reflection phase at a desired frequency. Consequently, AMC surfaces could be incorporated with on-chip antennas to act as: (1) a shield for the antenna from the silicon substrate and (2) a reflector that enhances the antenna radiation characteristics.

In previous reports [9] and [10], the AMC ground plane has been located below the silicon substrate as depicted in Fig.1(a). In this case, substrate waves can still be excited by the silicon substrate, since the AMC surface acts only as an antenna reflector and not as a shield. In this work, we tackle this problem by using the bottom metal layer embedded in the oxide as the AMC ground plane as shown in Fig.1(b). Furthermore, a folded dipole antenna is designed in the top metal layer above the AMC. The proposed folded dipole antenna shows a broadside radiation i.e. substrate waves do not distort the antenna radiation pattern with a gain of 2 dBi, which enables a true efficient system on-chip.

II. DESIGN AND SIMULATION

A. AMC Reflecting Surface

In order to design an AMC reflecting surface, a unit cell approach in Computer Simulation Technology Microwave Studio (CST-MWS) is used. The proposed AMC structure is comprised of a square-loop PRS on top of a thin oxide layer with a ground underneath as shown in Fig.2(a). The dimensions of the square-loop PRS are optimized to get a good compromise between increasing the AMC bandwidth ($f_{AMC} \pm 90$ degrees) and reducing the ohmic losses [11].

Periodic Boundary Conditions are applied along the XY Plane, and a floquet port is placed in the Z-direction at a distance of one wavelength above the surface. The de-embeded reflection phase is shown in Fig.2(b), where it is clear that the phase is zero at 94 GHz with a bandwidth of 2 GHz.

Fig. 2: (a) unit cell simulation model and (b) AMC Reflection phase, $D=0.6$ mm, $L=0.595$ mm, and $S=0.23$ mm.

B. AMC based On-Chip Dipole Antenna

In order to determine an actual AMC ground plane size, a half-wavelength dipole antenna is simulated on top of the optimized AMC structure as depicted in Fig.1(b) and is excited with a lumped port between its arms. Fig.3 depicts the maximum gain versus the number of AMC unit cells i.e. the AMC reflecting surface size. It is apparent that the gain increases with the increase in the number of unit cells, however the gain starts to compress as the number of unit cells exceeds 4×4 .

Fig. 3: Peak gain of a dipole antenna versus the number of AMC unit cells.

To gain insight into the advantages of using an AMC surface, Table I lists the impedance and radiation characteristics of a half-wavelength dipole, designed to resonate at 94 GHz, without (exposed to Si with $L_{dipole}=0.73$ mm) and with the 4×4 optimized AMC surface ($L_{dipole}=0.58$ mm). First, it is worth mentioning that without the AMC surface, the antenna radiation pattern is completely distorted by the spurious radiation due to the excited surface waves. Second, the AMC surface reduces the equivalent loss-resistance ($R_{loss} = R_{metal} + R_{dielectric}$), which leads to an increase in the radiation efficiency as well as the IEEE-Gain (antenna gain taking into account material losses). Third, it boosts the directivity at boresight, which when combined with the input resistance results in a realized gain of 4.74 dBi and a total

efficiency of 45%, respectively. This study illustrates that the AMC surface works as both a shield and a good reflector.

TABLE I: Impedance and radiation characteristics at 94 GHz of a half-wavelength dipole antenna

Property / Metric		Si	Ring-AMC
Impedance	Input Impedance $R_{in}(\Omega)$	49	15.6
	Loss-resistance $R_{loss}(\Omega)$	19.73	3.1
	Radiation-Efficiency (%)	22.7%	60%
	Directivity at boresight (dBi)	-3.2	8.3
	Gain-IEEE at boresight (dBi)	-9.8	6.2
Combined	Total-Efficiency (%)	22.2%	45%
	Realized-Gain at boresight (dBi)	-9.8	4.74

At resonance, the AMC-based dipole shows an input resistance of 15Ω , which is small compared to the characteristics impedance of conventional differential feeding transmission lines. This complicates the matching and limits the antenna bandwidth as previously presented in [13]. In order to increase the dipole input resistance, its folded version is designed. The relationship between the folded and dipole input impedances can be approximated as [14]: $(Z_{in})_{folded} \approx N^2 \times (Z_{in})_{dipole}$, where N is the number of dipole antennas. Based on the above equation, a folded dipole antenna with $N=2$ is simulated with the 4×4 AMC reflecting surface. At 94 GHz, the input resistance of the folded dipole is about 75Ω , which is about 4.5 times that of the dipole antenna.

C. AMC based Integrated Folded Dipole Antenna

The AMC backed folded dipole antenna is simulated with a planar feeding network comprised of a transition from a grounded CPW (to model testing the prototype with $150 \mu\text{m}$ GSG probes) to a microstrip line and a balun as shown in Fig.4. The simulation model is composed of three metal layers that are embedded inside the oxide layer, which resides on a thick silicon substrate. The first two metal layers (M1 and M2) are dedicated to the AMC reflecting surface, while the antenna and its feeding network are designed on the third top layer. The simulated S-parameters (shown in Fig.6) indicates

Fig. 4: Simulation model of the integrated AMC backed folded dipole antenna:(a) top view, (b) cross-sectional view, (c) planar feeding network.

that the antenna is matched from 92.3 GHz to 96.7 GHz i.e.

the antenna has a relative bandwidth of 4%. Moreover, the simulated radiation patterns in E and H planes are depicted in Fig.7. It can be observed that there is a squint in the main beam direction to about 30 degrees. This squint is not present in the radiation pattern of a directly fed AMC backed folded dipole antenna. Moreover, this squint exists in the H-plane, which is the feeder plane but not in the E-plane. This suggests that the squint is caused by spurious radiation from the feeding network. Finally, the gain at boresight is plotted against frequency (as depicted in Fig.8), where it is clear that the gain starts to increase as the frequency approaches the AMC reflecting surface bandwidth and reaches its peak value of 3.3 dBi at $f_{AMC} = 94$ GHz. Beyond this frequency, the gain starts to drop in value.

III. MEASURED RESULTS AND ANALYSIS

A. Prototype Fabrication

The fabrication process is carried out using our in-house cleanroom facilities using standard Si substrate and undergoing CMOS compatible steps as follows. First, the bottom metal layer (M1) is deposited by sputtering 15 nm of titanium (Ti), which act as a seed layer for 500 nm of gold (Au). Second, Plasma Enhanced Chemical Vapor Deposition (PECVD) technique is used to realize the first silicon oxide layer. Third, the positive tone ECI 3027 Photo-Resist (PR) is spin-coated, exposed to UV-light through a dark field mask, and developed for 60 seconds in MIF-AZ726 developer. Forth, the second metal layer is sputtered, which has the same material configuration and thickness as in step 1. Fifth, lift-off process is done, where the wafer is dipped in acetone and ultrasound sonication is applied. Sixth, the second layer of oxide is deposited via PECVD. Finally, steps 3 to 5 are repeated for the third metal layer, the fabricated prototype is shown in Fig.5.

Fig. 5: Surface electron microscopy images of the fabricated prototype:(a) top view, (b) cross-sectional and (c) M3 layer.

B. Impedance and Radiation Measurements

First, the antenna's input reflection coefficient is measured as shown in Fig.6. It is clear from the figure that the antenna is well matched with a return loss of $|S_{11}| \approx -21$ dB at 94 GHz. The measured reflection coefficient follows the same trend as the simulated one however, there is a slight shift in the frequency spectrum that originates from tolerance in

the relative permittivity of the deposited PECVD-based SiO_2 , which is confirmed by the post measurement simulations with $\epsilon_r=3.8$. Second, the antenna radiation characteristics are investigated, where a near-field to far-field W-band anechoic chamber is used. Taking into account the tolerance in the relative permittivity, Fig.7 compares the antenna simulated patterns having $\epsilon_r=3.8$ against the measured patterns at 96 GHz. In the E-plane, a good correlation is observed between the measured and simulated E-plane patterns of both co and cross polarized fields. Although there is also a good match between the co polarized simulated and measured fields in the H-plane, the measured cross polarization levels are 5-10 dB higher. It is believed that the reason behind this is the spurious radiation coming from the probe tips or the antenna radiation that is scattered by the probe body. This effect is more pronounced in the H-plane, since it is plane containing the probe. Furthermore, the measuring theta range across the H-plane is limited by the probe mounting base.

Fig. 6: Measured and simulated reflection coefficients.

Fig. 7: Normalized co and cross fields of measured (dashed lines) and simulated (solid lines) radiation patterns at 96 GHz: (a) E-plane and (b) H-plane.

The measured intrinsic peak-gain, at boresight, is found to be -1.4 dBi, which is less than the expected value from simulations. There are several possible mechanisms that could be responsible for the lower gain/increased losses, such as the overestimation of the metal conductivity. In order to have an estimate on the conductivity of the sputtered gold, the average conductivity of the top metal layer is measured using four-point probe method and is found to be 2.2×10^7 S/m. The measured conductivity is about half that of bulk gold (4.6×10^7 S/m), which was considered in the initial simulations. Furthermore, the cross-sectional SEM images shown

in Fig.5 shows that the bottom layer, which is titanium (Ti), is about 234 nm instead of the planned thickness of 15 nm, while the top layer, which is gold (Au), is about 144 nm. Considering that Ti has a much lower conductivity of $2.3 \times 10^{+6}$ S/m, the overall effective conductivity of the two-metal stack is expected to be near their average of about $(0.2+4.1) \times 10^{+7} / 2 = 2.2 \times 10^{+7}$ S/m; this is actually close to the results of the four-point probe conductivity measurement. The end-to-end AMC-backed on-chip folded dipole antenna is re-simulated with the actual Ti/Au metal thicknesses. As expected the inclusion of the thick low conductivity Ti-layer resulted in a substantial drop in antenna gain of 3.7 dB relative to the initial simulation result. After extracting this additional Ti-layer loss, the response of the actual peak-gain over frequency is plotted in Fig.8, where peak-gain increases gradually with frequency until it reaches 96 GHz, then it tends to decrease with further increase in frequency. This trend is attributed to the zero reflection phase property of the AMC reflecting surface which enhances the antenna radiation around f_{AMC} . Similar to the impedance measurement, the shift in f_{AMC} is due to the tolerance in ϵ_r of the deposited PECVD oxide layer, which is confirmed by a good match between the measured response and post-measurement simulation with $\epsilon_r = 3.8$. Finally, it is worth mentioning that even in presence of the extra losses from the Ti-layer, the antenna shows a peak-gain of -1.4 dBi, which is one of the highest reported gain among the on-chip antennas utilizing reflectors as gain enhancement technique at mm-wave frequencies as shown in Table II.

Fig. 8: Antenna peak gain against frequency for simulated cases of $\epsilon_r=4$ and $\epsilon_r=3.8$, and measured cases without and with the additional Ti-losses.

IV. CONCLUSION

In this paper, we present an on-chip folded dipole antenna backed with an AMC surface at 94 GHz. The fabricated prototype shows a peak intrinsic gain of -1.4 dB, which is 8 dB higher than without the AMC surface. The proposed AMC surface is completely embedded in the oxide layer, and hence it acts as both a shield from Si and a good reflector. The proposed approach has the advantage that it does not require neither an off-chip component nor complicate the fabrication process, however it requires a thicker oxide layer of $40\mu\text{m}$.

TABLE II: Comparison of mm-wave on-chip antennas using a reflector (PEC/AMC) as a gain enhancement technique

Reference	Antenna Type	Reflector	Frequency (GHz)	Bandwidth (GHz)	Gain (dBi)
[7]	Elliptical slot	GND	90	86-89	-5.7 0.7*
[9]	Circular loop	AMC GND below Si	60	57-67	-4.4
[10]	Leaky wave	GND	94	85-90	-2.5
This work	Folded dipole	AMC GND above Si	94	90-100	-1.4

*Gain using an off-chip $400\mu\text{m}$ thick quartz superstrate on top of the antenna

The authors envision that the numerous wireless applications at mm-wave frequencies will drive the silicon industry to include thicker oxide in their stack-ups to realize efficient radiators. This solution is cost effective and is analogous to the silicon industry including thicker metal layers in their fabrication processes to fulfill the demand of high quality factor on-chip inductors for efficient on-chip filters, matching networks, VCOs, and amplifiers.

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