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Planar heterojunction perovskite solar cell based on CdS electron transport layer

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ABSTRACT

We report on planar heterojunction perovskite solar cells employing a metal chalcogenide (CdS) electron transport layer with power conversion efficiency up to 10.8%. The CdS layer was deposited via solution-process chemical bath deposition at low-temperature (60°C). Pinhole-free and uniform thin films were obtained with good structural, optical and morphological properties. An optimal layer thickness of 60 nm yielded an improved open-circuit voltage and fill factor compared to the standard TiO₂-based solar cells. Devices showed a higher reproducibility of the results compared to TiO₂-based ones. We also tested the effect of annealing temperature on the CdS film and the effect of CdCl₂ treatment followed by high temperature annealing (410°C) that is expected to passivate the surface, thus eliminating eventual trap-states inducing recombination.

1. INTRODUCTION

Thin-film solar cells based on hybrid organic-inorganic perovskite absorber have emerged as one of the promising candidates for high-efficiency and low-cost solar cells, and have rapidly become competitive with existing thin-film technologies at laboratory scale. The fascinating aspect of organometallic perovskite solar cells (OPSCs) is that it just took 2-3 years to reach what other thin-film technologies achieved in 20 years of development, i.e. power conversion efficiency (PCE) recently approaching 20 % [1]. Perovskites have a combination of remarkable properties such as high absorption coefficient, high carrier mobility and long charge carrier diffusion lengths, exceeding 1 μm in mixed halide perovskites ($\text{CH}_3\text{NH}_3\text{PbI}_{3-x}\text{Cl}_x$) [2]. With these particular characteristics, high power conversion efficiency (PCE) is not limited to nanostructured or mesostructured heterojunctions, it can also be achieved using planar structures [3-5] with effective charge generation and separation. Moreover, this geometry provides a simplified approach for large scale integration of OPSCs.

The common OPSC configuration consists of sandwiching the perovskite absorber between an electron transport layer (ETL) and a hole transport layer (HTL) to respectively transfer the electrons and holes to the electrodes. In the conventional device structure, the perovskite material is infiltrated into a mesoporous TiO_2 layer deposited on top of a thin compact titania layer. This TiO_2 -based structure (mesoporous-compact) derived from dye sensitized solar cells (DSSCs), has been widely used in high efficiency OPSC and is commonly fabricated by solution-process followed by high temperature annealing (500 $^\circ\text{C}$) to achieve a good quality compact layer and an optimized scaffold for maximum charge collection. 2,2',7,7'-tetrakis(N,N-di-p-methoxyphenylamine)-9,9'-spirobifluorene (spiro-MeOTAD) has been mainly used as HTL in state-of-the-art high efficiency cells. It is believed that the charge carrier layers have significant impact on charge separation and carrier recombination at both top and bottom contacts. Recently, considerable effort has been devoted to replace both layers, ETL and HTL, with new materials that offer the possibility of low-cost and large-scale fabrication while maintaining high efficiency. TiO_2 has been extensively utilized in many applications such as dye-sensitized solar cells (DSSCs), photocatalysis and lithium-ion batteries. However, obtaining good quality TiO_2 at low-temperature remains still challenging, and even at high annealing temperatures TiO_2 does not provide a sufficient reproducibility necessary for solar cells applications. ZnO has been used as alternative ETL to TiO_2 and achieved remarkably high efficiency in planar structure devices [5], but the poor chemical stability of ZnO remains the main issue [6]. As an excellent substitute of TiO_2 one can quote SnO_2 that, thanks to its stability and the high electron mobility allowed the fabrication of highly efficient OPSC [7, 8]. Low temperature processed

amorphous WO_x was also used as ETL achieving device performance totally comparable to TiO_2 [9]. Attempts to use organic-based ETL have been successful too, Malinkiewicz *et al.* obtained high performance inverted structure OPSC with organic ETL and HTL [10] and at last, Kelly *et al.* demonstrated that high efficiency cells (>14%) can be achieved even without using an ETL [11]. These observation prompts further exploration of ETL materials, preferably deposited using an easy-to-implement technique that can lead to high efficiency cells.

Cadmium sulfide (CdS) is one of the most common metal chalcogenide materials which have been extensively explored in the last few decades due to its interesting optical and electrical properties. CdS was successfully used as the window layer in high efficiency thin-film solar cells based on cadmium telluride (CdTe) and copper indium gallium selenide ($\text{CuIn}_x\text{Ga}_y\text{Se}_2$). Although CdS can be deposited using various dry and wet methods, chemical bath deposition (CBD) is an attractive simple technique that can yield highly stoichiometric thin films with excellent uniformity and without pinholes. It is worth noting that TiO_2 and CdS have similar electron mobility which is found to be close to $5 \text{ cm}^2 \text{ V s}^{-1}$ for TiO_2 and between 1 and $10 \text{ cm}^2 \text{ V s}^{-1}$ for CdS [12, 13]. A Sputtered CdS film has been suggested as ETL in a mesoporous Al_2O_3 -scaffolding structure to replace the compact TiO_2 in OPSC [14]. However, the device exhibited a very poor power conversion efficiency of 1.53%. Hydrothermal-synthesized CdS nanorods array have been used as ETL in perovskite solar cells with maximum power conversion efficiency of 8.36% [15]. Recently, Liu *et al.* investigated an all-low temperature processed perovskite solar cells using CdS as ETL grown by solution process and achieved an efficiency of 11.2% [16], while, even more recently, Peng *et al.* reported a champion device efficiency of 15% [17]. Further to CdS, also CdSe was successfully used as HTM in OPSC, where 11% efficiency was obtained by depositing CdSe from colloidal quantum dots dispersion [18]. This further confirms that this class of materials, namely chalcogenides, can be effectively used as HTM in OPSC.

Here, we present a planar heterojunction perovskite solar cell based on a cadmium sulfide electron transport layer grown at very low-temperature (60°C) using a chemical bath deposition process on ITO and FTO substrates. Furthermore, the effects of CdS thickness, temperature post-annealing of CdS films, surface passivation and DI water cleaning of the surface of CdS films on device performance were extensively examined.

The light harvesting material used for the devices was methylammonium lead iodide $\text{CH}_3\text{NH}_3\text{PbI}_3$ and doped Spiro-OMeTAD was selected as HTL, both of which were deposited using solution-based process (spin coating). The measured devices reached efficiency as high as 10.8 % under 1 sun illumination. This promising result demonstrates the potential of using a simple thin film CdS

solution process in a planar OPSC structure. Moreover, this offers the opportunity to explore an extended family of other metal chalcogenide materials. Finally, although the liquid waste management is an issue, the CBD process is well suited for large-scale production and requires less investment than a vacuum process. In addition, this low-temperature solution process approach enables the use of flexible polymeric substrates, another possibility to make it more scalable and further reduce the production costs.

2. EXPERIMENTAL

Materials: all materials were used without purification. Anhydrous dimethylsulphoxide (DMSO), γ -butyrolactone (GBL), ethanol, diethyl ether, methylamine, 57 wt% hydroiodic acid in water, 4-tert-butylpyridine (TBP), anhydrous acetonitrile, anhydrous chlorobenzene, and lithium bis(trifluoromethane-sulfonyl)imide (Li-TFSI) were purchased from Sigma-Aldrich, whereas 99.999 % lead iodide (PbI_2) purchased from Alfa Aesar. Tris(2-(1H-pyrazol-1-yl)-4-tert-butylpyridine)cobalt(III) bis(trifluoromethylsulphonyl)imide (FK 102 Co(III) TFSI Salt) were purchased from Dyesol. 2,2',7,7'-tetrakis(N,N-di-p-methoxyphenylamine)-9,9'-spirobifluorene (Spiro-MeOTAD) 98% was purchased from Borun Chemicals, Methylammonium iodide (MAI) were synthesized in accordance with the literature [19, 20] $\text{CH}_3\text{NH}_3\text{PbI}_3$ was prepared by reacting the synthesized $\text{CH}_3\text{NH}_3\text{I}$ and PbI_2 at 1:1 molar ratio in 1 ml GBL/DMSO (3:2 Vol/Vol ratio) at 60 °C for 12 h.

Device fabrication and characterization: patterned tin-doped indium oxide ($R_s=12 \text{ } \Omega/\text{sq}$) and fluorine-doped tin oxide substrates ($R_s=15 \text{ } \Omega/\text{sq}$) were first scrubbed with dilute Extran 300 detergent solution to remove organic residues before immersing in an ultrasonic bath of dilute Extran 300 for 20 min. Samples were rinsed in flowing deionized water for 5 min before being sonicated (Branson 5510) for 10 min each in successive baths of acetone and isopropanol. Next, the samples were dried with nitrogen before being exposed to UV-ozone plasma for 10 min. CdS was prepared by CBD at 60°C with different deposition times on ITO and FTO substrates. In a typical CBD experimental procedure, 145 ml DI H_2O , 20 ml of 0.015 M CdSO_4 , 25 ml ammonia and 10 ml of 1.5 M thiourea solution were loaded into the reactor just before the substrates were inserted. The reaction was carried out under gentle stirring. After deposition, substrates were rinsed with DI H_2O and dried with N_2 . Lead perovskite solution was deposited onto CdS/ITO(FTO) substrates by a consecutive two-step spin-coating process at 1000 rpm and 4000 rpm for 10 s and 40 s, respectively. During the second spin-coating step, the films were flooded with chlorobenzene (100 μl) to promote crystallization then the samples were annealed at 80°C for 10 min. The HTM solution was coated on $\text{CH}_3\text{NH}_3\text{PbI}_3/\text{CdS}/\text{ITO}(\text{FTO})$ at 2200 rpm for 30 s. Finally, the samples were placed in a thermal

evaporator for evaporation of 100 nm of gold electrodes at $2 \text{ \AA} \cdot \text{s}^{-1}$ and pressure less than 1×10^{-7} Torr. The HTM solution was prepared by dissolving 80 mg of spiro-MeOTAD in 1 ml of chlorobenzene alongside 28.8 μL TBP, 17.6 μL Li-TFSI stock solution (520 mg Li-TFSI in 1 ml acetonitrile) and 29 μL FK 102 Co(III) TFSI Salt stock solution (300 mg FK 102 Co(III) TFSI Salt in 1 ml acetonitrile).

J-V measurements of solar cells were performed in the glovebox with a Keithley 2400 source meter and an ABET Technology Sun 3000 class AAA solar simulator calibrated to 1 sun, AM1.5 G, with a NREL calibrated reference silicon cell (ABET Technology). The external quantum efficiency (EQE) measurements were performed at zero bias by illuminating the device with monochromatic light supplied from a xenon arc lamp in combination with a dual-grating monochromator. The number of incident photons on the sample was measured for each wavelength by using a NIST calibrated silicon photodiode.

Films characterization: scanning electron microscopy (SEM) images were taken at 5 V accelerating voltage and beam aperture 30 μm , using a Zeiss Auriga microscope equipped with in-lens detector. Atomic force microscopy (AFM) scan was measured with Dimension Icon from Veeco on $1 \times 1 \mu\text{m}$ surface areas. The structure of the films was investigated by X-ray diffraction (XRD) Bruker D8 Discovery with Cu K α radiation source ($\lambda = 1.5418 \text{ \AA}$) and Raman spectroscopy in back-scattering geometry using a NT-MDT Ntegra setup equipped with diode laser with wavelength 532 nm as the excitation source and Peltier cooled Andor iDus CCD. UV-Vis-IR absorption measurements were taken using a Cary 6000i from Varian equipped with a diffuse reflectance accessory (integrating sphere). Samples were positioned at the center of the sphere and tilted of 20° with respect to the incident light beam. This configuration allows most of the specular and diffused reflected and transmitted light to be integrated in the sphere and measured by the detector with minimal losses. Photoelectron spectroscopy in the air (PESA) was measured using a PESA spectrometer model AC-2 from Riken Keiki, equipped with deuterium lamp as UV light source.

3. RESULT AND DISCUSSION

3.1 Influence of CdS thickness on the device performance

Figure 1: The architecture (a), cross-section SEM image (b) and energy band diagram of the as-fabricated device (c).

Figure 1 shows the device structure (a and b) and the bands alignment (c) of the planar heterojunction perovskite solar cell. The ionization potentials (IPs) of CdS, $\text{CH}_3\text{NH}_3\text{PbI}_3$ and spiro-MeOTAD were determined to be -6.16 eV, -5.36 eV and -5.24 eV respectively (Figure 2) by using photoelectron spectroscopy in air (PESA). The band gap of CdS and $\text{CH}_3\text{NH}_3\text{PbI}_3$ were estimated from the measured absorption spectra to be 2.35 eV and 1.59 eV respectively (Figure 8 and Figure 4). The corresponding energy diagram of ETL, HTL and absorber shows a favorable energy level alignment for electron extraction and hole blocking Figure 1 (left).

Figure 2: PESA spectra of (a) CdS film, (b) Methyl ammonium lead triiodide perovskite, and (c) doped Spiro-MeOTAD deposited on ITO substrate.

The CdS films were grown on patterned ITO or FTO substrates in a pre-heated bath at 60°C of 20 ml of 0.015 M CdSO_4 , 25 ml of NH_4OH (30%) and 10 ml of 1.5 M thiourea mixed in 146 ml DI water. The morphology of the as-prepared CdS films deposited on ITO is investigated by SEM and represented in Figure 3a. Atomic force microscopy (AFM) measurements show that the CdS layer has a very

smooth and compact morphology with mean roughness of 5.6 nm (Figure 3(b) and (c)). The $\text{CH}_3\text{NH}_3\text{PbI}_3$ perovskite absorber film was formed on top of the CdS layer by spin coating a solution of $\text{CH}_3\text{NH}_3\text{I}$ and PbI_2 and then annealed at 80°C for 10 min. Spin-coating of spiro-MeOTAD acting as the hole transport layer followed by thermal evaporation of the Au top electrode complete the device fabrication.

Figure 3: (a) $1 \times 1 \mu\text{m}$ AFM top view, (b) roughness of CdS film measured by AFM and (c) SEM top view.

We have first investigated the effect of the CdS thickness on the device performance. Solar cells were fabricated with CdS grown with various bath deposition times (10, 12.5 and 16 min) and keeping other parameters such as temperature and concentration constants. From cross-section SEM images

(not shown) the thicknesses of the CdS layers were estimated to be 40.00 ± 10 nm, 60.00 ± 10 nm and 110.00 ± 10 nm for 10 min, 12.5 min and 16 min deposition times respectively.

Figure 4: UV-Vis spectrum of $\text{CH}_3\text{NH}_3\text{PbI}_3$ film on glass annealed at 80°C for 10 minute.

Results in Figure 5(a) showed that the best PCE was obtained with a ~ 60 nm CdS layer deposited for 12.5 min. We note that this is twice the thickness of what was reported recently in another work. [16, 17] A thicker CdS film absorbs too much incident light and it also introduces a large series resistance, thus reducing J_{sc} and FF while a thin layer might lack of uniformity and presents some pinholes lowering the shunt resistance and thus the devices performances. The current density-voltage (J-V) characteristics of the different cells fabricated with different CdS thicknesses are shown in Figure 5(a).

Figure 5: (a) J-V curve of the different cells fabricated with different CdS thicknesses. (b) EQE of the best device, where CdS is deposited on ITO for 12.5 min.

The short-circuit current (J_{sc}), open-circuit voltage (V_{oc}), fill factor (FF) and PCE were determined to be $16.8 \text{ mA}\cdot\text{cm}^{-2}$, 1.05 V, 61% and 10.8%, respectively for the best cell fabricated with CdS deposited

for 12.5 min. In Figure 5(b), is shown the EQE spectrum of the best device (12.5 min), exhibiting spectral sensitivity ranging from the visible to the near-IR region (400 to 800 nm) with a peak IPCE of $> 80\%$. An expected EQE loss below 550 nm is observed from the EQE spectrum due to the low transmittance of CdS below this wavelength.

3.2 Influence of CdS annealing treatment

The effect of annealing treatment on thin-film CdS and CdS-based perovskite solar cells was also investigated. A comparative study was carried out with different kind of CdS layers: as deposited and annealed at 100°C , 150°C , 200°C under N_2 atmosphere. All devices were prepared by depositing a CdS layer with the optimized deposition time (12.5 min) on patterned ITO/glass substrates. The photovoltaic parameters of the different CdS-based cells are summarized in Table 1. As a reference, we used the champion compact TiO_2 -based cell was showing a maximum efficiency of 9.1%. A statistical study of efficiencies measured from 25 CdS-based devices shows an average PCE of 9.51%. Furthermore, the average efficiency of TiO_2 -based devices, fabricated with the same criteria of the CdS-based ones ($\text{CH}_3\text{NH}_3\text{PbI}_3$ and spiro-MeOTAD deposition) is stuck at about 6% and with much higher number of faulty devices. The improvement compared to the TiO_2 based devices lies mainly in the FF and V_{OC} values. This can be attributed to the excellent electron transport/extraction properties of CdS and to the CdS/ $\text{CH}_3\text{NH}_3\text{PbI}_3$ interface with better characteristics that reduces the series resistance. Also, the improved FF can be assigned to a lower interfacial recombination originated by a lower defectivity of CdS with respect to TiO_2 .

Figure 6: SEM images of CdS films deposited on ITO substrates: (a) as-deposited, (b) annealed at 100°C , (c) annealed at 150°C and (d) annealed at 200°C . DI water sonicated CdS films: (e) as-deposited, (f) annealed at 100°C , (g) annealed 150°C and (h) annealed at 200°C .

We observed that CdS-based devices showed reduced performances when annealed, mainly in the J_{SC} and FF compared to the untreated samples. Therefore, it was found out that the annealing

treatment did not improve the efficiency and instead introduced a large series resistance when the temperature was increased from 100°C to 200°C.

Table 1. The efficiency of CdS-based devices according to different parameters such as thickness, annealing temperature and surface treatment.

ETL	Thickness (nm)	T annealing under N ₂ (°C)	J _{sc} (mA.cm ⁻²)	V _{oc} (V)	FF (%)	PCE (%)
			Average Champion cell	Average Champion cell	Average Champion cell	Average Champion cell
CdS	60	None	17.027	1.081	53.5	9.5
			17.392	1.055	58.5	10.7
CdS	60	100	15.153	1.053	45.6	7.3
			15.511	1.033	47.4	7.6
CdS	60	150	14.951	1.043	45.2	7.1
			15.123	1.050	46.2	7.2
CdS	60	200	11.293	0.913	29.2	3.1
			11.802	0.904	32.0	3.7
CdS	60	100/DI cleaning	16.112	1.087	44.6	7.8
			16.231	1.086	45.2	8.0
CdS	60	150/DI cleaning	15.469	1.023	48.3	7.6
			15.574	1.031	48.3	7.7
CdS	60	200/DI cleaning	13.097	1.035	30.6	4.2
			13.254	1.031	31.3	4.3
TiO ₂	50	500	17.717	0.987	52.2	9.1

To understand the effect of annealing on the device performances, we first looked at the morphology of the annealed and as-deposited CdS layers using SEM. In Figure 6(a), SEM image of the as-deposited CdS thin-film surface shows a uniform and compact film. However, after annealing, we notice the presence of flakes and heterogeneities randomly distributed on the surface, which gradually increased with the annealing temperature (Figure 6(c) and (d)).

As reported in Table 1, devices with CdS that underwent a thermal treatment have unexpectedly poorer performances than devices with pristine CdS film. We thought that the flakes probably made of CdO, act as recombination sites resulting in current and fill factor depletion. Indeed, J_{sc} and mostly FF decrease at higher rate than V_{oc} , indicating that the loss of efficiency although there is also an increase of the series resistance is mainly due to interfacial recombination. For that reason, an ultrasound treatment in DI water was carried out to remove the surface flakes. The obtained surface shown in Figure 6(g) and (h) is uniform and similar to the as-deposited sample. One can notice that there is no increase in the grain size after annealing and the roughness of the films did not change as well. The DI water ultrasonic cleaning shows improvement in the device performance for the annealed samples. However, although after this treatment the efficiency of annealed CdS-based devices is higher than their counter part fabricated without DI water cleaning, the as deposited CdS-based devices still result in the best efficiency, Figure 9. Observing the J-V characteristics of annealed CdS devices, it can be noticed that further to an increase of series resistance a shunt component is also introduced. This can be caused by the formation of cracks in the CdS film after the annealing process that can create current leakage channels from the $CH_3NH_3PbI_3$ layer to the ITO electrode.

XRD patterns of as-deposited and 200°C-annealed CdS thin-films are reported in Figure 7(a). The peaks of the hexagonal or cubic phases cannot be distinguished since the three main peaks at 26.8°, 44.3° and 52.5° can be attributed either to (111), (220), (311) planes of the cubic structure or to (002), (110), (200) planes of the hexagonal structure [21]. It is reported that CdS grows in the cubic structure at low temperature but a phase transformation into hexagonal phase can be completed when CdS is annealed or grown at temperature higher than 75°C [22]. From XRD spectra, similar full width at half maximum (FWHM) for the peaks of the as-deposited and annealed samples indicate no improvement in the crystalline quality of the film after annealing, which is in good agreement with the SEM images showing no increase in grain size (Figure 6). Besides, no secondary or oxide phases (CdO) are observed for CdS annealed under N_2 atmosphere. Conversely, devices featuring CdS films annealed in air show much lower efficiency, probably due to the formation of a CdO layer causing an enhanced recombination.

As a complementary technique to XRD, typical Raman spectra of as-deposited and N₂-annealed CBD-CdS films are illustrated in Figure 7(b). The two well-defined lines at 303 cm⁻¹ and 600 cm⁻¹ correspond to the first-order scattering (1LO) and second-order scattering (2LO) of the longitudinal optical modes of CdS respectively. The FWHM and peak intensity ratio of 1LO/2LO that depends on the strength of electron-phonon interaction, are not changing with annealing temperature (inset of Figure 7(b)), which indicates that no increase of the grain size occurred in this case. Although the I_{1LO}/I_{2LO} ratio is influenced by the grain size and crystallinity, it has been shown to be independent of the CdS structure [23]. However, the straightforward increase in intensity with annealing temperature of both 1LO and 2LO modes can be explained by a potential phase transformation in the CdS structure or at least a structure disorder. Indeed, it has been reported that CdS thin films deposited by CBD adopt a metastable cubic structure [22]. Hence, a phase transformation toward the hexagonal structure can be thermally activated during annealing. The phase transformation of CdS may entail a lattice mismatch with the light absorber. In fact, CH₃NH₃PbI₃ adopts a cubic structure (space group Pm3m, Z = 1) with lattice constant in the range $a_0 = 6.26 - 6.29$ Å, which is relatively similar to cubic CdS ($a_0 = 5.82$ Å) as compared to tetragonal TiO₂ ($a_0 = 3.74$ Å). By switching progressively to the hexagonal phase of CdS (wurtzite, $a_0 = 4.14$ Å) when annealing, we obtain a larger mismatch between the lattice constants of CH₃NH₃PbI₃ and CdS, which can explain the detrimental properties of annealed CdS in this case and their negative impact on the device performance.

Figure 7: thin film XRD (a) and Raman spectra (b) of CdS films annealed at different temperatures.

Absorption spectra of the CBD-deposited CdS films before and after annealing are presented in Figure 8. We observe a slight red-shift of the absorption edge with the increase of annealing temperature, which indicates a decrease of the bandgap from 2.38 to 2.30 eV. These results are in good agreement with other studies showing a decrease of the bandgap for a transformation from

cubic to hexagonal phase [24]. This induces a higher absorption in the visible range when the annealing temperature increases, negatively affecting the device performances.

Figure 8: UV-Vis spectra of as-deposited and different temperatures annealed CdS films.

3.3 High temperature CdCl_2 treatment of CdS films

Further to the heat treatment applied with maximum temperature of 200°C that did not improve the performances of the cells, we investigated the impact of CdCl_2 treatment along with a following heat treatment at higher temperature (410°C). For these experiments, the 60 nm (12.5 min) CdS film was deposited on patterned FTO because of its far better resilience to heat treatment in terms of sheet resistance preservation compared to ITO. Moreover, we applied a CdCl_2 coating by dipping the samples in saturated CdCl_2 solution in water for different times followed by annealing at 410°C in air for 15 min. The color of CdS films changed from yellow to orange-yellow after annealing. This treatment is known to improve the structural and electrical properties of CdS in CdTe solar cells [25]. The beneficial effects of the CdCl_2 treatment of the CdS/CdTe heterojunction are well known in terms of grain growth, reduced interface recombination, increased carrier collection and reduced number of defect states at or near the CdS/CdTe interface. In order to investigate and then to control the influence of CdCl_2 treatment, we compared the efficiencies of different cells treated with different dipping time and then annealing at 410°C under O_2 for 15 min.

Figure 9: J-V curves of CdS-based devices, where CdS was annealed at different temperatures.

As shown in Table 2, the highest device efficiency (7.7%) for CdCl₂-treated samples was obtained after 10 min annealing. This is still lower than the 10.3% PCE obtained for as-deposited CdS deposited on FTO without annealing or CdCl₂ treatment. SEM images (Figure 10) show that some particles are present on the surface of the CdS film, which may act as traps for charge carriers. Also, there might be some degree of partial oxidation of the CdS surface due to the annealing in air. Those features can lead to the lower fill factor and eventually lower PCE (Figure 9).

Figure 10: SEM images of CdS films a) before CdCl₂ treatment and b) after CdCl₂ treatment.

To examine the influence of CdCl₂ treatment at a crystalline structure level, a Raman investigation of the films was performed. Results indicate that CdCl₂ treatment slightly improved the crystallinity of CdS films (Figure 11). Also, The CdS was annealed at 410°C for 15 min without treatment, and the as-fabricated devices gave 5.3% efficiency (Table 2).

Figure 11: Raman spectra of CdS films before and after CdCl₂ treatment.

Thus, CdCl₂ treatment, similarly to CdTe/CdS devices [25], could in theory improve the device efficiency by preventing oxidation of CdS at higher temperature and to obtain a better crystallinity. However, as mentioned before, the high annealing temperature used (410°C) promotes the phase transformation from cubic to hexagonal that has a higher lattice mismatch with CH₃NH₃PbI₃ thus causing a possible bad interfacial contact and consequently a higher series resistance.

Table 2. Device characteristics of perovskite solar cells with CdS ETL before and after CdCl₂ treatment.

CdCl ₂ treatment time (min)	Annealing Condition and T(°C)	J _{SC} (mA·cm ⁻²)	V _{OC} (V)	FF (%)	PCE (%)
0	As-dep	17.337	1.055	56.1	10.3
5	Air, 410	16.395	0.973	38.5	6.1
10	Air, 410	15.840	0.968	49.9	7.7
15	Air, 410	13.984	0.910	31.8	4.0
0	Air, 410	15.325	0.932	37.4	5.3

4. CONCLUSIONS

Uniform CdS film was deposited on ITO and FTO using a low-cost and scalable CBD method and near 11% PCE was obtained for both ITO and FTO based devices. Optimum CdS film thickness of 60 nm

was determined based on the device performances and it was shown that temperature annealing does not lead to any improvement of the device efficiency. CdCl_2 treatment can improve device performances compared to the sole annealing but the ultimate efficiency is still lower than as-deposited CdS film devices. Moreover, device performance can be further improved through device optimization by controlling interface and band gap tuning of CdS by doping. In conclusion, we demonstrated that a metal chalcogenide can be used instead of TiO_2 showing high stability, reproducibility and a better scalability of the low temperature deposition method that can be extended to other chalcogenides and applied even to flexible substrates.

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Notes

The authors declare no competing financial interest

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Planar heterojunction perovskite solar cell based on CdS electron transport layer**Highlights**

- Chemical bath deposition of cadmium sulfide
- Chalcogenide (CdS) based electron transporting layer
- Lead halide perovskite solar cell
- Thermal and chemical treatment of CdS layer