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Transparent Flash Memory using Single Ta₂O₅ Layer for both Charge Trapping and Tunneling Dielectrics

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ABSTRACT: We report reproducible multibit transparent flash memory in which a single solution-derived Ta₂O₅ layer is used simultaneously as charge trapping and tunneling layer. This is different from conventional flash memory cells, where two different dielectric layers are typically used. Under optimized programming/erasing operations, the memory device shows excellent programmable memory characteristics with a maximum memory window of ~10.7 V. Moreover, the flash memory device shows a stable 2-bit memory performance, good reliability, including data retention for more than 10⁴ sec and endurance performance for more than 100 cycles. The use of a common charge trapping and tunneling layer can simplify advanced flash memory fabrication.

1. INTRODUCTION

Among several non-volatile memories available on the market, flash memory is the leading product in semiconductor non-volatile memory industry. This is largely due to its simple one transistor device structure.¹⁻³ Moreover, the compatibility with existing complementary metal–oxide–semiconductor (CMOS) processes, multi-bit per cell storage capability, and higher chip density makes flash memory one of the most promising next-generation nonvolatile memories.⁴⁻⁶ The conventional flash memory device consists of a floating gate (islands of polysilicon in the modified gate stack) structure in a metal-oxide-semiconductor-field-effect transistor. In these devices, by controlling the applied bias on the control gate, charge carriers can be stored in the floating gate layer, which is usually isolated from the semiconductor channel by a thin layer of dielectric material (tunneling layer).⁷ Meanwhile, the consumer demands for low-cost and high-density storage devices is pushing the physical scaling in floating gate flash memory devices. However, these scaling efforts have reached their physical limit due to the floating gate coupling issue, which arises from the neighboring cells coupling caused by the gate capacitance and gate leakage current due to reduced tunnel oxide thickness.^{8,9} In the meantime, charge trapping flash (CTF) type memory devices (replacing floating gate by a charge trapping layer, such as Si_3N_4) are free from the gate coupling issue due to their advantageous structure. They are forecast to become alternative candidates to continue vertical scaling of flash memory devices.^{10,11} However, the conventional CTF memory devices suffer from a trade-off between program/erase (P/E) ability and data retention time. If the thickness of tunnel oxide is thinner than 3 nm, a long data retention time over ten years may not be achieved due to the stress-induced leakage current (SILC).¹² On the other hand, multibit memory per cell is an urgent requirement for existing memory technology to increase memory capacity. Conventionally, the existing flash memories available on the market consist of only two memory states, either high (ON) or low (OFF), which store binary data (0 and 1). A realization of

several stable intermediate states between ON and OFF states may lead to the multibit memory operations.¹³

To overcome these issues, flash transistor memory devices with high dielectric constant materials (high- k) such as TiO_2 ,¹⁴ HfO_2 ,^{15,16} and CrO_2 ,¹⁷ have been proposed as charge trapping layer (without the tunneling layer) to improve flash memory performance. One of the main advantages of using high- k materials is the fact that high- k materials can act as charge trapping layer as well as tunneling dielectric layer at the same time; this fact enhances the program efficiency without the need for an additional tunneling layer. Also, high- k materials can be engineered with higher trap density and sufficiently large bandgap offset with the oxide semiconductor layer (such as ZnO) which leads to further improvement in device performance.¹⁸ Among several high- k materials, Tantalum pentoxide (Ta_2O_5) is one of the promising materials as a charge trapping layer in CTF type memory devices. This is due to its high dielectric constant, higher charge trapping capability due to the presence of large amount of oxygen vacancies which act as electron trap center, good thermal and chemical stability.¹⁹ Also, a moderate band gap of ~ 4.4 eV and high band offsets with oxide semiconductors make it as a promising candidate for the charge trapping flash memory applications.^{20,21} A wide variety of preparation techniques have been used so far for the preparation of Ta_2O_5 thin films, including chemical vapor deposition (CVD), atomic layer deposition (ALD), sputtering, etc. However, the preparation of Ta_2O_5 by solution process is attractive because it is simple and inexpensive deposition process, with great potential for large-area production. Several research groups have already reported different chemical routes for the preparation of Ta_2O_5 precursor solution for the spin coating of Ta_2O_5 films.²²⁻²⁴ However, to the best of our knowledge, the charge trapping capability of solution-processed Ta_2O_5 has never been used in non-volatile CTF memory applications. Therefore, it is necessary to investigate the charge trapping property of solution processed Ta_2O_5 and its impacts on the flash memory performances.

Herein, we report a transparent multi-bit flash memory realized with Ta₂O₅ thin film as charge trapping layer prepared by solution process and used in a thin film transistor (TFT) memory device configuration. Widely used n-type semiconductor ZnO is used as channel material due to its high mobility and stable electrical performance. As a blocking oxide layer, *i.e.*, gate oxide layer, Al₂O₃ is used due to its high band gap and insulating properties. ITO is used as a bottom gate, and source/drain (S/D) contact.

2. EXPERIMENTAL SECTION

2.1. Preparation of Ta₂O₅ precursor solution. In this study, Ta₂O₅ was prepared from Tantalum (V) chloride (TaCl₅, analytical grade, 99.99% pure) powder obtained from Sigma-Aldrich following the chemical route proposed by M. Epifani *et.al.*²² The complete preparation of the Ta₂O₅ precursor solution was done inside of a glove box filled with N₂. The preparation of the solution starts with 1 gm of TaCl₅ with which 10 ml of methanol was added slowly in a pre-cleaned glass vial. The reaction was carried out for one hour. After that, DI water was added dropwise into the solution maintaining the molar ratio of water to Ta as 16:1 followed by stirring for 24 hours. After stirring for 24 hours, 30 mg of cetyltrimethylammonium bromide (CTAB) was added to improve Ta₂O₅ film uniformity and its adhesion. After adding CTAB, the solution was further stirred for another 24 hours to complete the process. Finally, the solution was used for spin coating after keeping it for next two days inside the glove box.

2.2. Device fabrication and characterizations. The CTF type memory devices studied in this work were fabricated on commercially purchased ITO coated glass substrates, where ITO acts as an electrode for bottom gate thin film memory transistor configuration. The gate oxide, Al₂O₃ and channel semiconductor layer, ZnO was deposited by ALD technique, knowing the advantage of ALD technique for the preparation of pinhole-free oxide layers with controlled thickness and large area uniformity at low temperature. Both Al₂O₃ and ZnO was deposited at 160 °C chamber

temperature, and deionized water (DI) was used as the source of oxygen. Trimethylaluminum (TMA) and Diethylzinc (DEZ) were used as the ALD precursor for the deposition of Al_2O_3 and ZnO respectively. Total 800 cycles of TMA and 160 cycles of DEZ was used to achieve the desired thickness of about 80 nm for Al_2O_3 and 25 nm for ZnO layers. The pulse/purge times (in second) for Al, Zn, and O sources used in the device fabrication are 0.015/10, 0.02/10, and 0.015/10 respectively.

The device fabrication process starts with the cleaning of indium-tin-oxide (ITO) coated glass substrates sequentially with acetone, 2-propanol, and DI water in an ultrasonic bath for about 5 min each and then dried by the N_2 gas flow. The cleaned ITO/glass substrates were then used for the deposition of Al_2O_3 thin film following the ALD technique described above. After the deposition of Al_2O_3 thin film, oxygen plasma treatment was carried out on the substrate to make the Al_2O_3 surface hydrophilic. After that, the Ta_2O_5 precursor solution was spin coated on the oxygen plasma-treated several Al_2O_3 /Glass substrates using a 0.2 μm PTFE filter at a rotation speed of 6000 rpm for 30 sec. The wet film was then kept on a hot plate at 90 $^\circ\text{C}$ temperature for 15 min for drying. After cooling down the sample to room temperature, spin coating using the same recipe was repeated to achieve a uniform Ta_2O_5 thin film with the desired thickness. Finally, the films were annealed in a tube furnace for one hour at different temperatures, such as 100, 200, 300, 400 and 500 $^\circ\text{C}$ to obtain the Ta_2O_5 film for further process. After that, the semiconductor layer, ZnO was patterned by photolithography and wet etching using buffered oxide etchant, 7:1 (J.T. Baker). A bilayer of Ti (~5 nm)/ITO ~80 nm) was used as source/drain (S/D) layer which was patterned by photolithography followed by a lift-off process. Ti and ITO films were deposited by using e-beam evaporation and sputtering system respectively. To study the impact of Ta_2O_5 film thickness on the memory performance, different memory devices were prepared with different rotation speeds of 2000 (~40 nm), 3000 (~32 nm), 4000 (~25 nm) and 5000 (~22 nm) rpm for 30 s followed by annealing at 400 $^\circ\text{C}$ for 1 hours. Also, we prepared reference TFT devices without a Ta_2O_5 layer,

keeping all other layers identical. These devices without Ta₂O₅ layer will henceforth be called as TFT-A. The TFT memory devices prepared with a rotation speed of 6000 rpm for 30 sec and annealed at 400 °C will, henceforth, be called as TFT-B. Finally, all devices were annealed at 160 °C for one hour using a hot plate in air. The thicknesses of different films were measured by a surface profilometer (Veeco Decktak 150). The x-ray diffraction (XRD) patterns of the Ta₂O₅ films were obtained using a Bruker D8 Advance X-ray diffractometer equipped with Cu K α radiation. The chemical composition and the structural analysis of Ta₂O₅ films were performed using X-ray photoelectron spectroscopy (XPS). XPS studies were carried out in a Kratos Axis Ultra DLD spectrometer equipped with a monochromatic Al K α x-ray source ($h\nu=1486.6$ eV) operating at 150 W, a multichannel plate and delay line detector under a vacuum of $1\sim 10^{-9}$ mbar. UV-vis transmittance spectra were measured by Evolution 600 UV-VIS Spectrophotometer (Thermo Scientific). The source and drain electrodes with channel width to length ratio (W/L) of 5 (W=500 μ m and L=100 μ m) were used for the electrical measurements. Current-voltage characteristics were measured using a Keysight B1500A semiconductor device analyzer in combination with a semi-automatic probe station from Cascade Microtech. Capacitance-voltage curves were measured using an Agilent E4980A Precision LCR meter.

3. RESULTS AND DISCUSSION

3.1 Material Characterizations. The chemical composition and structure of the spin coated Ta₂O₅ film was investigated using X-ray diffractometry (XRD) and X-ray photoelectron spectroscopy (XPS) techniques. Figure 1a shows XRD patterns obtained from Ta₂O₅ films annealed at different temperatures ranging from 100 to 500 °C. It can be seen that the films remained amorphous up to 200 °C and that some crystalline peaks start appearing from 300 °C. However, the Ta₂O₅ film annealed at 500 °C shows several peaks. Major peaks are identified at 33.4°, 33.98°, 46.6° and 48.03° correspond to the (012), (280), (004), and (-421) crystal planes, respectively. For

our optimized memory devices, we used polycrystalline type Ta₂O₅ films annealed at 400 °C as the charge trapping layer.

The XPS spectra obtained from the Ta₂O₅ films annealed at 400 °C are shown in Figure 1b and Figure 1c. The binding energies were corrected for the sample charging effects using the C 1s line at 285 eV. All XPS spectra were deconvoluted using the standard Gaussian-Lorentzian function. However, before deconvolution of all spectra, Shirley background correction was applied to eliminate background signals. Figure 1b shows Ta 4f core level spectra with two distinct peaks corresponding to the Ta 4f_{7/2} and Ta 4f_{5/2} at 26.4 and 28.29 eV, respectively, where spin-orbit splitting between Ta 4f_{7/2} and Ta 4f_{5/2} photoelectrons was found to be about 1.89 eV. This value reflects the strong binding between tantalum and oxygen atoms, which is in good agreement with the previously reported XPS results by several other groups.^{25,26} These two peaks represent the characteristics of Ta–O bonding.²⁷ The Ta 4f spectrum shows a small and broad peak at 22.5 eV with a negligible intensity that forms a tail at the lower energy side of the main peak, which is characteristic of metallic Ta.²⁸ These results indicate that the spin-coated film at the surface is very close to the stoichiometric Ta₂O₅ with a small amount of non-oxidized Ta. The O 1s XPS spectra obtained from the Ta₂O₅ film can be fitted with three components. The main peak at 530.5 eV corresponded to the O 1s core level of the O²⁻ anions and referred to the Ta-O chemical binding.²⁹ Whereas, a relatively small peak at higher binding energy side (at 532.02eV) corresponds to the surface contamination and may be due to the presence of C=O.³⁰ However, the intermediated peak at ~530.8 eV is necessary for proper fitting, and is attributed to the oxygen vacancies present in the film. It was found that the surface contamination in the Ta₂O₅ film decreases with increasing annealing temperature. However, oxygen vacancies increase up to 400 °C and then decreases again at 500 °C. The O1s XPS spectra obtained from Ta₂O₅ films annealed at 100, 200, 300 and 500 °C are shown in Figure S1a to Figure S1d) respectively. The comparison of the areal percentage of C=O contamination and oxygen vacancies are shown in Table S1 (Supplementary Information

File).

UV-VIS transmittance spectra measured with a film stack containing all four layers on glass substrates as used in memory transistor (ITO (Gate)/Al₂O₃ (gate oxide)/Ta₂O₅ (Charge trapping layer)/ZnO (Semiconductor)/Ti/ITO (Source/Drain)) are shown in Figure 1d. It is found from the UV-VIS spectra that the entire stack of layers in the Flash device exhibits about 65% of transparency in the whole visible range of the electromagnetic spectrum. Hence, the flash memory devices used in this study can be considered as the semi-transparent memory device. The transparency decreases due to the use of Ti interlayer. However, the use of Ti is necessary to get a stable memory device performance. The schematic 3-D device structure that used in this study is shown inset of Figure 1d. The memory transistor prepared with a bottom gate and the top contacts nonvolatile memory devices with a Ta₂O₅ thin film layer as the charge trapping layer.

3.2 Electrical Characterizations. To investigate the performance of the flash memory, we studied TFT devices without (TFT-A) and with (TFT-B) Ta₂O₅ charge trapping layer. The typical output characteristics of the n-channel (ZnO) TFT devices (TFT-A) with respect to different gate bias are shown in Figure 2a. Transfer characteristic curves were measured in both forward and backward sweep of the gate voltage at a constant drain voltage of 10 V is shown in Figure 2b. In the gate sweep voltage ranges (-5V to 15 V to -5V), the TFT-A device shows negligible hysteresis in the transfer characteristics. The reference TFT-A device showed $I_{\text{on}}/I_{\text{off}}$ ratio of $>10^6$, low subthreshold swing values of ≈ 380 mV/dec and very low gate leakage current of $\approx 10^{-11}$ A, as indicated by the dotted line in Figure 2b. Next, to check the memory operation in the TFT-A, the device was programmed with gate-to-source voltage (V_{GS}) of 35 V for 2 ms keeping the source and the drain grounded. It can be observed that a negligible shift (0.6 V) of threshold voltage (V_{th}) can be achieved from TFT-A type transistors, as shown in Figure 2c. Therefore, almost negligible charging and/or discharging of the charge carriers occurs at the semiconductor/gate dielectric interface for the reference TFT devices which have no extra charge trapping layer. The absorbed

water molecules may form such interfacial traps at the semiconductor/gate dielectric interface leading to V_{th} instability under programming/erasing operation. These results indicate that a charge trapping layer is necessary for the flash memory devices operation.

The TFT device containing Ta_2O_5 (~18 nm) as charge trapping layer (TFT-B) was also measured under the same bias conditions used to test the TFT-A device. The output characteristics obtained from the memory transistor in its initial or virgin stage (without applying any programming or erasing operations) are shown in Figure 2d. It can be observed that the memory device shows good linear behavior at a low drain voltage and a good saturation region behavior at a high drain voltage, as well. The typical transfer characteristics obtained from the memory transistor is shown in Figure 2e. A small hysteresis of ~0.7 V with high I_{on}/I_{off} ratio of $>10^7$, low subthreshold swing values of ≈ 500 mV/dec and very low gate leakage current of $\approx 10^{-11}$ A are obtained. The saturation mobility (μ_{sat}) was calculated to be around $7.21 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, which is comparable to previously reported TFT devices with Al_2O_3 as gate dielectric and ZnO as a channel layer.³¹ Here, it may be noted that there was no charging effect while the transfer curve was measured in the double sweep mode of the gate to source bias when there was no program/erase operation. However, standard flash memory performance obtained from the memory transistors (TFT-B) after proper program/erase operation, as shown in Figure 2f. The memory window (ΔV_{th}), is defined as the shift of V_{th} with respect to the applied program/erase bias pulses (*i.e.*, $\Delta V_{th} = V_{th}(\text{Programmed}) - V_{th}(\text{erased})$). In contrast, after applying the programming (35 V for 2 ms) and erasing (-40V for 4 ms) bias to the gate terminal, keeping source and drain as grounded, we obtained a maximum memory window of ~10.7 V. We also checked the memory performance using different device dimensions (different W and L values) and found little effect on the maximum memory window, as shown in Figure S3 (see the supplementary section). Initially, the memory window increases by increasing programming/erasing bias. However, after applying sufficiently high bias pulses as mentioned in both programming/erasing operations, V_{th} reached certain saturated values and maintained these

values even under the application of higher bias. In general, the shifting of V_{th} , *i.e.*, the increase/decrease of trapped charges in the charge trapping layer is realized by applying higher programming or erasing pulses. Initially, when the programming bias was low, the charge trapping process in the Ta_2O_5 layer was random. However, with increasing gate programming bias, the number of trapped charges in the Ta_2O_5 layer increases which lead to the enhanced Coulombic repulsion which caused the saturation in V_{th} .^{6,13} In this study, the V_{th} was calculated from the intercept of the plot of $\sqrt{I_D}$ vs. V_G . During the application of the positive bias stressing on the bottom gate electrode, electrons could be injected from the ZnO semiconductor layer and are stored in the Ta_2O_5 charge trapping layer. As a result, the V_{th} shifts in the direction of the positive voltage in comparison with the initial transfer curve, which further confirms the charge trapping nature of Ta_2O_5 layer. However, the stored electrons (negative carriers) in the Ta_2O_5 layer are ejected from the Ta_2O_5 layer and re-enter to the ZnO channel during the erasing operation, in which -40V was applied to the bottom gate for 4 ms, resulting in shifting of V_{th} in the direction of the negative voltage.

Next, we studied the effect of the Ta_2O_5 thickness on the memory performance. Specifically, we measured memory performance of the TFT-B type transistor devices with different Ta_2O_5 thickness, which was obtained by controlling spinning speed during the spin coating of Ta_2O_5 films. The memory performance obtained from the memory devices fabricated with four different thicknesses of 40, 32, 25 and 22 nm are shown in Figure S4 (a-d), respectively. It is observed that a memory window of 1.85, 2.61, 4.67, and 5.45 V, respectively, can be achieved with different Ta_2O_5 thickness after applying same P/E bias conditions that were used for TFT-B type devices. These results signify that the thinner charge trapping layer results in better memory performance. This result may be due to the fact that the electric field is higher across the thinner Ta_2O_5 films. Hence the injection and release of carriers from the charge trapping layer are easier. These results are in good agreement with the previously reported results by other research groups for similar type

devices.³² It should be noted that there is a limit to reducing the dielectric thickness in these devices since at some point, further decrease in thickness makes it impossible to store charge due to the charge leakage effects, which will cause poor retention performance. Hence, an optimized charge trapping layer thickness is necessary to achieve good CTF type memory performance.

Next, we demonstrate multibit memory performance after achieving a large memory window of ~ 10.7 V, which is believed to be sufficient for distinguishing different intermediate memory states.³³ By controlling the amount of stored charges in the charge trapping layer, one can achieve multiple memory states in a CTF type flash memory devices. Hence, to realize a multibit memory operation, a precise linear control on the threshold voltage (memory window, $\Delta V_{th} = |Q_t / C_{ox}|$, where Q_t is the total charge stored in the Ta₂O₅ charge trapping layer and C_{ox} is the gate oxide capacitance) is necessary by applying different programming and erasing biases. The multilevel memory performance obtained from our memory devices (TFT-B) is shown in Figure 3. Different amount of charge injection into the Ta₂O₅ layer can be successfully achieved by applying specific programming biases to the bottom gate electrode. A typical 4-state memory characteristic is shown in Figure 3a, after application of successive programming biases of 25, 30 and 35V for 2 ms each. Afterward, the device was erased using -40V bias for 4 ms. The resultant memory states labeled as “11”, “01”, “10” and “00” lead to the successful demonstration of 2-bit per memory cell performance (total non-overlapping threshold voltage (V_{th}) windows = 2^n , where n represents numbers of bits). It is needless to say that the well-controlled V_{th} that we obtained leads to various current levels to detect different electrical memory states, which reveals that the amount of charge carriers stored in the trap sites of Ta₂O₅ layer could be reversibly modulated by applying an external gate bias.³⁴

For a nonvolatile flash memory device, endurance and data retention capability are important performance parameters. Here, we have three programmed states (01, 10 and 00) and

one common erased state (11). Hence, we have three different memory windows, ΔV_{th} (V_{th} (programed) – V_{th} (erased)) available for the demonstration of multibit memory performance. Figure 3b shows the cyclic endurance performance of three different memory windows obtained from our memory devices after applying a continuous sequence of programming bias (1) – reading - programming bias (2)– reading - programming bias (3)– reading – erasing bias – reading process. It was observed that the device exhibits highly reproducible memory behavior with well-separated programmed/erased states for more than 100 cycles with little degradation. Total number of trapped charges in the Ta_2O_5 layer for each memory window was estimated to be $\sim 1.2 \times 10^{12} \text{ cm}^{-2}$, $\sim 2.7 \times 10^{12} \text{ cm}^{-2}$, and $\sim 3.8 \times 10^{12} \text{ cm}^{-2}$, respectively. On the other hand, data retention capability is one of the most important factors for flash memory applications, as it estimates the length of time the information can be stored in the memory device. The data retention characteristics of the memory devices were measured at room temperature and at 85 °C using the memory devices in the programmed/erased states, as shown in Figure S5 and Figure 3c, respectively. After changing the memory state by applying the proper biasing on the gate terminal, the data was read in 100 sec time intervals. It was found that at the room temperature measured values of memory windows fluctuated during measurement. However, the memory windows are found to be comparably more stable when measured at 85 °C, and decrease over time, which is related to the charge leakage process in the device. Possible charge loss mechanisms during the retention process typically depend on localized defect states in the charge trapping layer that provide leakage pathways through the blocking dielectric layer (Al_2O_3), and as well as leakage path to the semiconductor layer, each of which depends on film thickness and quality of the Ta_2O_5 layer.^{35,36} However, since the high-quality Al_2O_3 was used as blocking layer, the probability of charge leakage through it will be small. During the application of a high temperature of 85 °C, leakage of charges by the thermally activated electrons increased, and hence more charge loss was observed. However, the memory states were well-maintained for more than 10^4 sec. For a reliable multibit memory operation, it is

important that different memory states do not overlap with each other over time. By using the extrapolation method, it is expected that a maximum memory window of $\sim 7V$ can be preserved after ten years measured at $85^\circ C$. This remaining memory window is still large; making it is possible to distinguish between the programmed/erased states with reasonable sensing margins. To demonstrate the stability of the memory states with uniform process control, cumulative distribution of different memory states obtained from randomly selected ten identical memory devices were studied, as shown in Figure 3d. The cumulative distribution characteristics for the different devices indicate good process control and reliability for multibit data storage applications.^{37, 38}

In order to understand the charge transfer mechanism during the program and erasing process, schematics of the equilibrium energy band diagram for the flash memory devices under programming, storage and erasing states are shown in Figure 4a, Figure 4b, and Figure 4c respectively. It has been shown in the programming operation that the transfer curve, as well as the V_{th} , has shifted in the positive direction after applying positive program bias to the gate electrode. Hence, the Ta_2O_5 charge trapping layer acts as an electron trapping layer. The electrons get trapped in the Ta_2O_5 layer coming from the conduction band of the semiconductor, ZnO, during a programming operation when a positive bias is applied to the gate. It should be noted that a high conduction band offset of ~ 1.13 eV between Ta_2O_5 charge trapping layer and ZnO forms, which should ideally restrict charge flow through this interfacial barrier layer. However, when a sufficiently large programming bias is applied to the gate junction, a band bending at the conduction band of Ta_2O_5 is also expected. As a result, electrons from the ZnO layer will tunnel into the Ta_2O_5 layer following the Fowler-Nordheim (FN) tunneling mechanism. The band-bending increases with increasing programming bias and hence the probability of electron tunneling to Ta_2O_5 layer increases leading to more shifting of V_{th} towards the positive side. Few of these electrons may trap in the shallow trap centers, just below the conduction band edge of the Ta_2O_5 layer and most of them possibly trapped in the deep level trap centers. In this condition, if the

potential at the gate junction removed, the trapped electrons, particularly in the deep level, ideally remains forever, if there is no charge leakage. In fact, the trapped electrons in the deep traps need an energy of ~ 2.5 to 2.7 eV (which is the energy difference between the deep level trap energy and the conduction band energy of Ta_2O_5) to reach the conduction band of Ta_2O_5 for further leakage.^[39] Hence, after completing the programming process, the stored negative charges remain in the Ta_2O_5 layer and hold the programmed V_{th} state. However, practically, a small leakage is possible through the defects in the charge trapping layer. As a result, a small degradation in the retention characteristics was observed. However, the stored charges in the Ta_2O_5 charge trapping layer can be transferred back to the channel again during the application of erasing operation (negative bias) on the gate electrode. Under an application of the sufficiently large amount of negative bias to the gate terminal, trapped electrons inside the charge trapping layer gain enough energy to reach the conduction band of the Ta_2O_5 layer and then transfer to the channel layer through the band lowering at the interface. As a result, the negative carrier concentration in the n-type semiconductor channel increases leading to reducing the threshold voltage, as erased state. The repetitive operation of the program and erase method in the gate terminal of the flash memory device leads to flash memory operation.

4. CONCLUSION

In summary, transparent flash memory devices have been fabricated using solution-derived Ta_2O_5 as both charge trapping and tunneling. The memory window could be tuned by the thickness of the Ta_2O_5 charge trapping layer, and a maximum memory window of ~ 10 V was achieved. Moreover, endurance operation for more than 100 cycles and retention performance for more than 10^4 sec were achieved without much degradation, which indicates a good quality flash memory device. The fact that the Ta_2O_5 layer in this study acts as charge trapping layer as well as tunneling dielectric layer simplifies device structure and indicates that Ta_2O_5 prepared by solution processing is a promising material for future flash memory applications.

Figure 1:

Figure 1. (a) XRD patterns obtained from the spin coated (6000 rpm) Ta₂O₅ film annealed at different temperatures. XPS spectra obtained from the (b) Ta 4f and (c) O1s core level of the Ta₂O₅ film annealed at 400 °C. (d) UV–vis transmittance spectra of ITO/Al₂O₃/Ta₂O₅/ZnO/Ti/ITO films deposited on a glass substrate. The inset shows 3D schematic device structure used in this study.

Figure 2.

Figure 2. The (a) output, (b) transfer characteristics, and (c) the memory performance obtained from the reference TFT device without Ta₂O₅ film as charge trapping layer. The (d) output, (e) transfer characteristics, and (f) the memory performance obtained from the memory device with Ta₂O₅ film as charge trapping layer.

Figure 3.

Figure 3. (a) The 2-bit memory performance obtained from our charge trapping TFT memory devices. The (b) endurance and (c) retention characteristics of the memory windows obtained from the multibit memory measurements. (d) The cumulative distribution of different V_{th} obtained from randomly selected ten devices.

Figure 4.

Figure 4. The schematic energy band diagram of the memory device in its (a) programmed, (b) storage, and (c) erased state conditions.

ASSOCIATED CONTENT

Supporting Information. O1s XPS spectra obtained from the Ta₂O₅ film annealed at 100, 200, 300 and 500 °C temperature; comparison of different components obtained from the O1s XPS spectra in tabular format; variation of capacitance with frequency of the ITO/Al₂O₃/Ta₂O₅/Ti/ITO structure; Maximum memory window variation with different W and L; flash memory performance for different Ta₂O₅ film thickness obtained from different spin coating speed; Memory retention performance at room temperature.

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Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Notes

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