Highly Manufacturable Deep (Sub-Millimeter) Etching Enabled High Aspect Ratio Complex Geometry Lego-Like Silicon Electronics

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Please submit a plain text version of your cover letter here. **If you are submitting a revision of your manuscript, please do not overwrite your original cover letter. There is an opportunity for you to provide your responses to the reviewers later; please do not add them here**.	26th May 2016 Dr. José Oliveira Editor, Small Wiley-VCH Dear Dr. Oliveira, Enclosed please find the Communications entitled “Highly Manufacturable Deep (Sub-millimeter) Etching Enabled High Aspect Ratio Complex Geometry Lego Like Silicon Electronics”. We presetn a novel deep reactive ion etching based highly manufacturable generic process using a hybrid soft/hard mask layer to etch up to 500 m with an aspect ratio over 100. This process allows easy and clean removal of metallic hard masks, preserves the high quality interface of underlying substrate, and endures during long duration etches. This technique enables “Lego” like integrated circuit (IC) chip placement on soft substrates for free-form (physically flexible, stretchable and reconfigurable) electronics. For example, we demonstrate functional heating elements and interconnected complex geometric features of Lego-like silicon on flexible platform. Moving forward, this work offers an effective highly manufacturable and economical alternate for sub-millimeter deep etching and formation of high aspect ratio features. The major advances reported in this manuscripts are: 1.A highly manufacturable CMOS compatible process for achieving high-aspect ratio Lego-like complex objects formation from silicon. 2.Compared to gold standard BOSCH or other relevant processes, this process shows record dimensions and cleanest process for high aspect ratio feature formation. 3.Demonstration of such silicon Lego electronics on flexible platforms. As reviewers we humbly suggest the following esteemed authorities: 1.Prof. Zhenan Bao – Stanford University, (zbao@stanfrod.edu) 2.Prof. Roger Howe – Stanford University (rthowe@stanford.edu) 3.Prof. Tsu-Jae King Liu – University of California, Berkeley (tking@eecs.berkeley.edu) 4.Prof. Jack Ma – University of Wisconsin, Madison (mazq@engr.wisc.edu) 5.Prof. David Clarke – Harvard University (clarke@seas.harvard.edu) 6.Prof. Mark Hersam – Northwestern University (m-hersam@northwestern.edu) Should you need any further information, please let me know. Thank you in advance, Sincerely yours, Muhammad

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Highly Manufacturable Deep (Sub-millimeter) Etching Enabled High Aspect Ratio Complex Geometry Lego Like Silicon Electronics

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Keywords: Lego, silicon electronics, deep reactive ion etching, soft/hard mask.

Formation of high aspect ratio Lego like silicon electronics can enable hybrid integration of diverse range of electronics on soft materials enabling free-form (physically flexible, stretchable and reconfigurable) electronics. In that regard, micromachining, used in complementary metal oxide semiconductor (CMOS) technology, microelectromechanical systems (MEMS), dynamic random access memory (DRAM) capacitors and through silicon vias (TSVs) for 3D Integrated Circuits (3D-ICs), can play effective role.[1,2] Many bulk micromachining techniques have been demonstrated in the past for making high aspect ratio structures.[3-7] The techniques generally utilize a hard mask (for example: metal) material to withstand abrasive deep reactive ion etching (DRIE).[4] Klaassen *et al.* reported a bilayer of silicon oxide and photoresist (PR) used as mask to form 300 μm deep trenches.[6] Aluminum and multilayer Nickel/Aluminum hard masks were also used to etch 200 μm deep trenches in silicon.[3,7] The deep etching ability has enabled bulk micromachining to fabricate micro-motors, electrostatic resonators, optical filters, micro-lenses, thermal actuators, MEMS switches, capacitive sensors and actuators, and lately flexible and stretchable electronic devices.[3, 6, 8-21]

The Bosch process is widely used for obtaining the smooth sidewalls required in DRIE for most applications.[22] The process is comprised of successive etching and deposition cycles

to passivate the sidewalls as etching progresses. The reactions that take place in Bosch process are:[23]

Main etching at the Si surface:

$$SF_6 + e^- \rightarrow SF_3 + 3F + e^- \quad (1)$$

$$Si_{(solid)} + 4F \rightarrow (SiF_4)_{(gas)} \quad (2)$$

Plasma polymerization at the sidewalls:

$$C_4F_8 + e^- \rightarrow 2\,C_2F_4 \rightarrow CF_2, CF_3, \ldots\ldots \quad (3)$$

$$C_2F_4, CF_2 \xrightarrow{\text{Ploymerize at Side Walls}} (CF)_x \quad (4)$$

Flexible electronic devices fabricated utilizing the Bosch process have already been demonstrated.[8,9,11,13,16,21] However, deeper trenches for stretchable electronics (through the whole thickness of Si (100) wafer) required a Titanium/Gold bilayer hard mask.[10] The use of hard masks during deep etching (hundreds of microns) imposes some manufacturing limitations. The first challenge is the choice of the hard mask material. The DRIE time is affected by the depth of the trenches as well as the lateral dimensions due to the micro-loading effect. The feature "conductance" is a measure of how easily reaction byproducts can be vented and reactant gases can be supplied for further etching. As the trench depth (and aspect ratio) increases, the collisions between the leaving and entering gases increase, dropping the etch rate.[24] Micro-loading results in drop in feature conductance. Narrower features suffer more because of the relative difficulty inherent in a smaller outlet/inlet trench.[3,6] The hard mask needs to be selective to the extremely long DRIE process so that the mask is not etched during the process, and at the same time it needs to be easy to remove after the deep etch is performed. For instance, Nickel is a widely used hard mask during the DRIE but it is extremely hard to remove and consequently forms NiSi with silicon when exposed to high temperatures. Alternatively, Gold can be used but it has stress mismatch induced adhesion issues and requires an underlying Titanium layer for adhesion. Moreover Gold is not

recommended because of its high diffusivity and cross contamination of silicon based electronics. Alternatively, Aluminum can be easily etched using metal RIE in Halide gases but it forms alloys with Silicon at the interface. In the case of wet etching, the whole wafer has to be immersed and there are contamination and selectivity issues that would not be suitable for CMOS flows, especially at an advanced stage after the devices are fabricated, to make flexible/stretchable, with the myriad materials involved as the solutions are highly acidic. Furthermore, the metal/silicon interface is degraded due to ions bombardment during sputtering deposition or diffusion if atomic layer deposition is used at an elevated temperature. Finally, even dry etching of hard mask involves plasma and DC power which detrimentally affect the surface roughness of Silicon or underlying interface.

To this end, we demonstrate a novel hybrid soft (sacrificial)/hard mask layer for DRIE of sub-millimeter structures. The devised process is generic and various sacrificial layers can be used. The technique does not affect the surface of the material under the hybrid mask, prevents diffusion and alloy formation between hard mask and underlying layers, and avoids the abrasive etching of the hard mask after DRIE. The generic flow is outlined in **Figure 1a**.

We used the hybrid dual layers mask to etch through the whole thickness of a Si (100) 4'' wafer (~500 μm). The main fabrication steps are depicted in Figure 1b. First, negative tone PR AZ 5214E with image reversal capability is spun. Pyrolysis bake is then carried out followed by broadband exposure, an image reversal bake, and a final flood exposure dose. This makes the complete PR layer insoluble in AZ 726 MIF developer. Next, a thin Aluminum layer is sputtered at room temperature followed by positive tone PR AZ ECI 3027 layer spinning and patterning. The Aluminum layer is patterned using the PR mask and metal RIE using inductively coupled plasma (ICP), Cl_2, BCl_3, and Ar mixtures at 80°C. Then, the negative tone PR is etched in O_2 plasma RIE followed by DRIE of Silicon. Finally, the hybrid dual PR/Al mask is removed by immersing in Acetone bath.

A similar approach has been followed using PR only mask and the maximum depth achieved was 100 µm. Figure 2a shows the depth profile using a Dektak profilometer. On the other hand, the hybrid PR/Al mask showed selectivity during etching of the whole silicon substrate (~525 µm).

To assess the effect of the new process on the etched features and the underlying silicon substrate surface, Zygo profiler measurements, for surface roughness, and scanning electron microscopy (SEM) imaging, for feature size measurements, were carried out. Figure 2b,(a) shows the results from surface morphology measurements of various substrates (scanned area ~500 x 500 μm^2). The results show that the surface of the substrate where only PR was used and etched during the DRIE process has the highest variations in height. This is a challenge when using PR, especially that the process does not have real time feedback to know when the PR is about to be gone and what is the maximum safe depth using specific PR types. On the other hand, using Al only hard mask and wet etching in Gravure or PR/Al hybrid mask and removal in Acetone showed closer results to pristine silicon surface. On a smaller scale, Figure 2c shows the surface roughness measurement using atomic force microscopy (AFM). As aforementioned, Gravure is strongly acidic and not recommended for wafers containing fabricated devices and structures, Figure 2,(d) shows the energy dispersive X-ray spectroscopy (EDX) results for 0.27 x 0.21 mm^2 area of the silicon sample surface exposed to Gravure exhibiting peaks for fluorine, and carbon residues.

Figure 3a shows the SEM images before removal of the hybrid PR/Al mask stack. The debris due to evident peeling of the hard mask in Figure 3a suggest that the PR underneath might have been etched around the exposed edges during the prolonged process causing the undercut that resulted in peeling off as well as the significant variations in the edge roughness. Figure 3b shows scaled illustrations of designed features and realized 500 µm deep features. The measurements confirm a slight increment in lateral features of few micro meters. This effect is more important when dealing with narrower features. For instance, the 6 µm extra

width in the 700 μm wide trench constitutes a distortion of less than 1%; whereas, for finer features and edges the variation is relatively more significant. Figure 3c suggests that there is a consistent growth in feature dimensions of few microns, independent of feature size. Figure 3d confirms the observation, as even the fine feature line (2 μm by design) resulted in ~5 μm realized line width. This means that for specific realized structure using the deep etch process, a scaled down design is required to account for the increase in dimensions during etching. The increase in dimensions is a result of the extended etching time and physical ions bombardment during the RIE, damaging the side walls of the mask. Noteworthy, the reported increase in dimensions is lateral from the top view which is different from the barreling effect (another optimization parameter concerned with the slight undercut in trenches for deep etch).[24] Due to the micro-loading effect, an extended etch was needed to make sure all features have been etched down to 500 μm. Deceleration in etching rates due to drop in feature conductance and loading has been modelled by Kiihamaki *et al.* for aspect ratios < 20 but is inapplicable for higher aspect ratios.[25] Therefore, exact required time and etching rates could not be predicted. Nonetheless, the hybrid mask persisted throughout the etch losing only the smoothness of the sidewalls (scalloping). The line edge roughness is an optimization issue that has been already extensively addressed. For instance, Song *et al.* used focused ion beam (FIB) milling for smoothing the sidewalls after DRIE to achieve a surface roughness of 5.7 ± 1.8 nm.[26] Kawata *et al.* demonstrated that introducing O_2 plasma to the DRIE process results in smoother sidewalls,[27] and Mukherjee *et al.* achieved 7 nm surface roughness on sidewalls also introducing O_2 into the DRIE chamber.[28] Pham *et al.* used tetramethylammonium hydroxide (TMAH) at 80°C to achieve a feature size of 2 μm and smooth sidewalls.[29] Smooth sidewalls/edges are critical for applications involving electronic transport as the rough edges would scatter electrons and reduce overall current. On the other hand, the roughened sidewalls might be useful for lateral actuators and switches where cantilevers are switched on/off by moving laterally (in-plane) because the roughness of the surface would

mitigate stiction problems and at the same time increase the electrostatic attraction due to the increased surface area. Furthermore, heat dissipation is a critical issue in miniaturized systems since scaled dimensions reduce the surface area available for heat dissipation. Hence, the increased surface area due to non-smooth edges can be utilized. Table 1 summarizes the results of the novel hybrid soft/hard mask DRIE using the PR/Al mask example in comparison with previous techniques used for extremely deep features.

The demonstrated deep etching would enable sub-millimeter etching structures, variations of regular etching enabled by choice of any hard mask without the requirement for later removal using strong chemicals or abrasive etching, highly customized dicing patterns (parallel process and can have customized curves and twists), supporting high-performance bulk mono-crystalline silicon modules on polymers for flexible systems, and is a step forward towards novel flexible packaging of high performance electronics (Figure 4).

Figure 5 shows the implementation of a representative novel packaging approach for regular and irregular dies using polymer encapsulation (PDMS). To examine the established contact using the flow in Figure 4b, Figure 5b shows the heating up of the embedded heater silicon die through the extended copper interconnects. The designed heater initial resistance was 1.7 kΩ. The resistance measured through the copper interconnects after embedding was ~2 kΩ, indicating an extra 300 Ω resistance, mainly due to ~150 Ω contact resistance at the two ends of the designed heater. Contact resistance improvements are subject for future exploration.

Figure 6 shows irregular dicing patterns using the hybrid soft/hard mask and DRIE to dice silicon pieces. Plasma dicing has been previously proposed and it has potential for replacing traditional mechanical dicing and predecessor laser dicing.[33] Noteworthy, the reported technique in current form is suitable for the suggested practical applications including novel packaging, dicing methodologies, and other applications where feature size is at least few tens of microns, such as MEMS switches. However, further optimizations to study

the effect of soft/hard mask total thickness, soft/hard mask thickness ratios, and investigating different tone PR order and other possible polymer variations should determine the true potential and limitations of the technique in terms of minimum attainable resolution (5.7 µm reported in this work) and the expected variation in edge roughness and feature widening (3-6 µm reported in this work).

In conclusion, we have demonstrated a novel deep reactive ion etching based highly manufacturable generic process using a hybrid soft/hard mask layer to etch up to 500 µm with an aspect ratio over 100. This process allows easy and clean removal of metallic hard masks, preserves the high quality interface of underlying substrate, and endures during long duration etches. This technique enables "Lego" like integrated circuit (IC) chip placement on soft substrates for free-form (physically flexible, stretchable and reconfigurable) electronics. For example, we demonstrate functional heating elements and interesting complex geometric features of silicon. Moving forward, this work offers an effective highly manufacturable and economical alternate for sub-millimeter deep etching and formation of high aspect ratio features.

Experimental Section

Designing the Hybrid Mask Stack:

We used the hybrid dual layers mask to etch through the whole thickness of a Si (100) 4'' wafer (~500 µm). Negative tone PR AZ 5214E with image reversal capability is spun at 3000 rpm for 30 seconds for a ~1.6 µm thick layer, then pyrolysis bake at 105°C for 2 minutes followed by broadband exposure at 90 mJ/cm^2, then an image reversal bake at 120°C for 2 minutes and ultra-violet flood exposure for 1 minute. This makes the complete PR layer insoluble in AZ 726 MIF developer. Next, a thin 200 nm Aluminum layer is sputtered at room temperature at 400 Watts, and 10 mTorr pressure and Argon plasma. Then, positive tone PR AZ 3027 was spun at 3000 rpm for 30 seconds and baked at 100˚C for 1 minute for a ~4 µm

thick layer and patterning using broadband 200 mJ/cm^2 constant dose and developed in AZ 726 MIF developer for 60 seconds. Then the Aluminum layer is patterned using the PR mask and metal RIE in three steps: (1) breakthrough etch using 10 sccm Cl_2, 40 sccm BCl_3, and 10 sccm Ar at 40 mTorr, 1500 Watts Inductively coupled plasma (ICP), 50 W RF at 80°C, (2) main etch using 40 sccm Cl_2, 10 sccm BCl_3, and 10 sccm Ar at 20 mTorr, 1500 Watts Inductively coupled plasma (ICP), 150 W RF at 80°C, and (3) overetch using 10 sccm Cl_2, 30 sccm BCl_3, and 10 sccm Ar at 40 mTorr, 1500 Watts Inductively coupled plasma (ICP), 50 W RF at 80°C. Then, the negative tone PR is etched in 50 sccm O_2 RIE at 50 mTorr, 1500 W ICP, 30 W RF at 20°C.

***Deep Etching Silicon*:**

Silicon DRIE was done using Bosch process of successive deposition and etching cycles using cryogenic cooling at -20°C for smooth sidewalls. The initial Ar plasma strike was executed using 10 sccm C_4F_8, 20 sccm SF_6, and 50 sccm Ar at 15 mTorr, 2000 W ICP and 20 W RF for 10 seconds. The deposition step was composed of 100 sccm C_4F_8 and 5 sccm SF_6 at 30 mTorr, 1300 W ICP, and 5 W RF for 3 seconds and the etching step was composed of 5 sccm C_4F_8 and 100 sccm SF_6 at 30 mTorr, 1300 W ICP and 35 W RF for 8 seconds. Since after the prolonged DRIE, the dies will be disconnected as Silicon connecting them is etched away, using a carrier wafer is necessary. We used a carrier wafer with half-baked ECI 3027 PR (30 pyrolysis bake instead of the full pyrolysis 60 seconds), then placed the wafer to be diced on top then continued the remaining 30 seconds pyrolysis bake. This fixes the dies after dicing in place and they are easily detached during the last step of hybrid mask removal as Acetone dissolves the ECI 3027 PR.

Removal of the Hybrid Mask Stack:

The hybrid mask is then easily removed in Acetone bath which dissolved the –ve tone AZ 5214E PR easily, which in turn was gone with all mask material on top similar to the lift-off process widely used.

Embedding the Silicon Heater Chip:

PDMS solution is first mixed with curing agent (ratio 10:1, respectively). The mixture is left to cure at ambient conditions. Porous cleanroom wipers (alternatively many other porous substrates can be used) are then used to support the extending interconnects. Ideally, for high resolutions, the interconnects can be sputtered and patterned on a flexible flat substrate. In our case, copper foil was used and glued using epoxy to the porous substrate. The stack composed of the porous substrate and copper interconnects is then applied to the semi-cured PDMS, and the silicon chip is flipped upside down and pressed against the stack in designated location such that the die's contacts coincide with the copper interconnects. Another PDMS capping layer is applied to protect and cover the silicon chip, and the whole setup is left to fully cure in ambient conditions.

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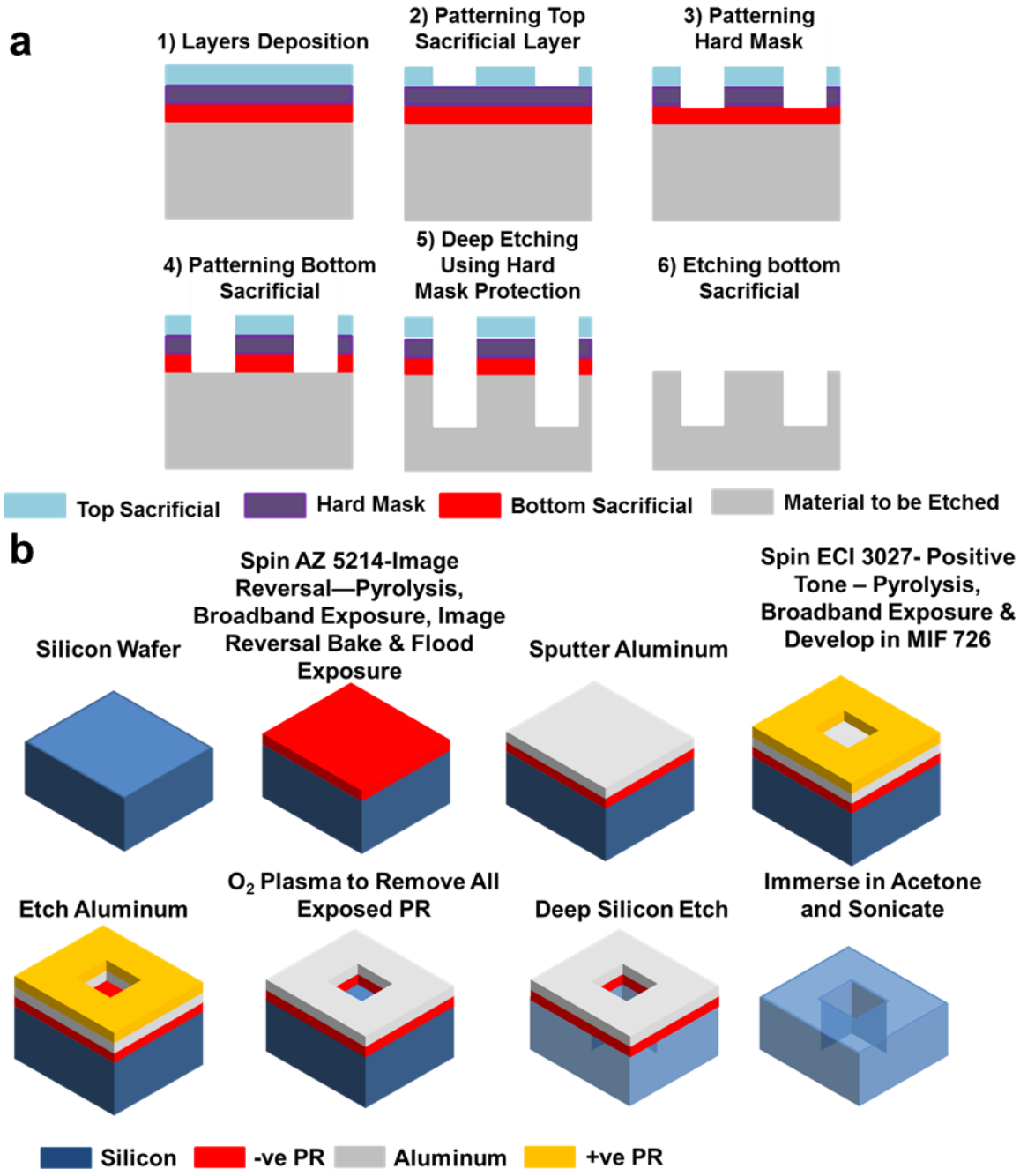

Figure 1. Generic process flow for the hybrid dual soft/hard mask deep etching (a), and fabrication flow using -ve PR/Al hard mask for deep etching of Si (100) (b).

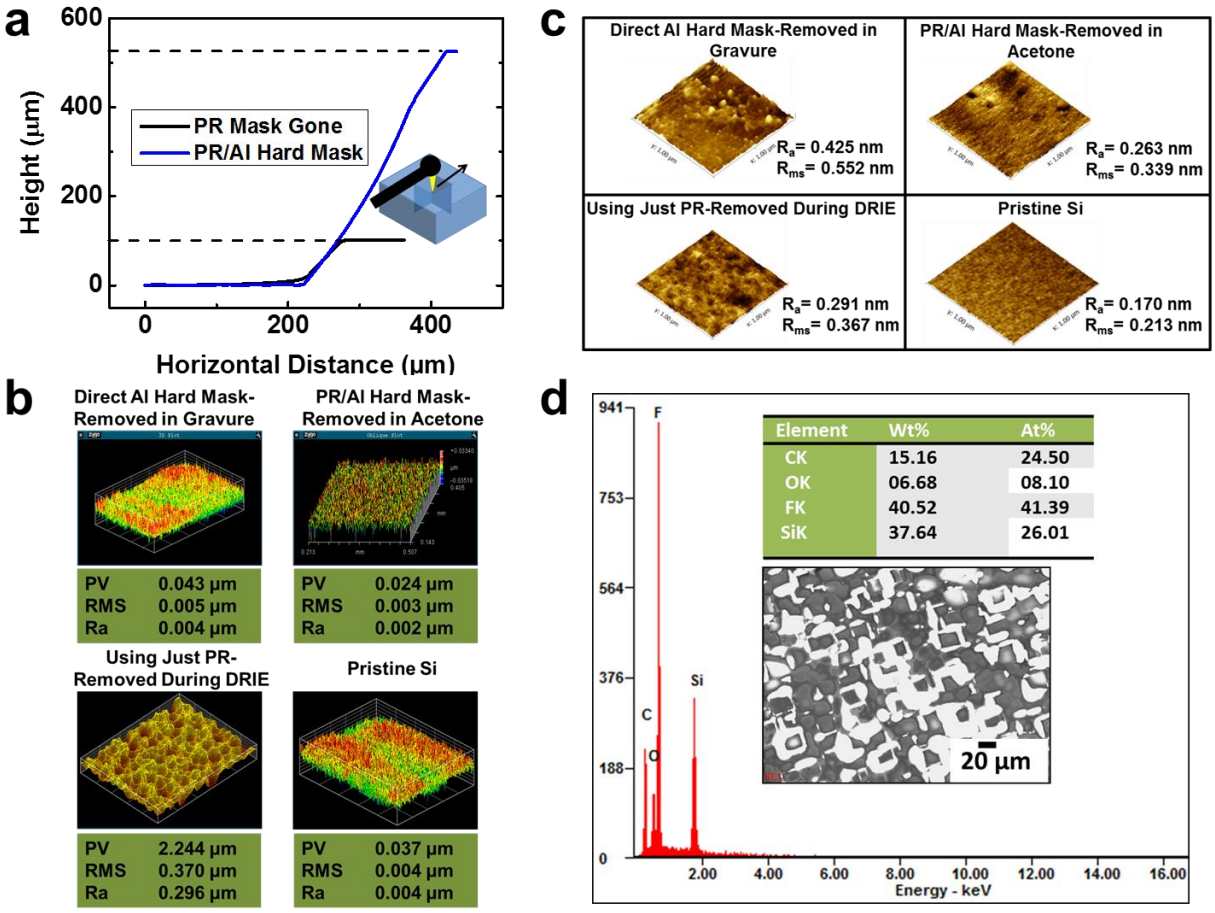

Figure 2. Profilometer measurements for the DRIE structure: (a) Zygo profiler surface morphology and maximum height (PV) for various substrates, (b) atomic force microscopy (AFM) surface roughness measurements for various samples, (c) and (d) energy dispersive X-ray spectroscopy (EDX) results for Gravure treated sample.

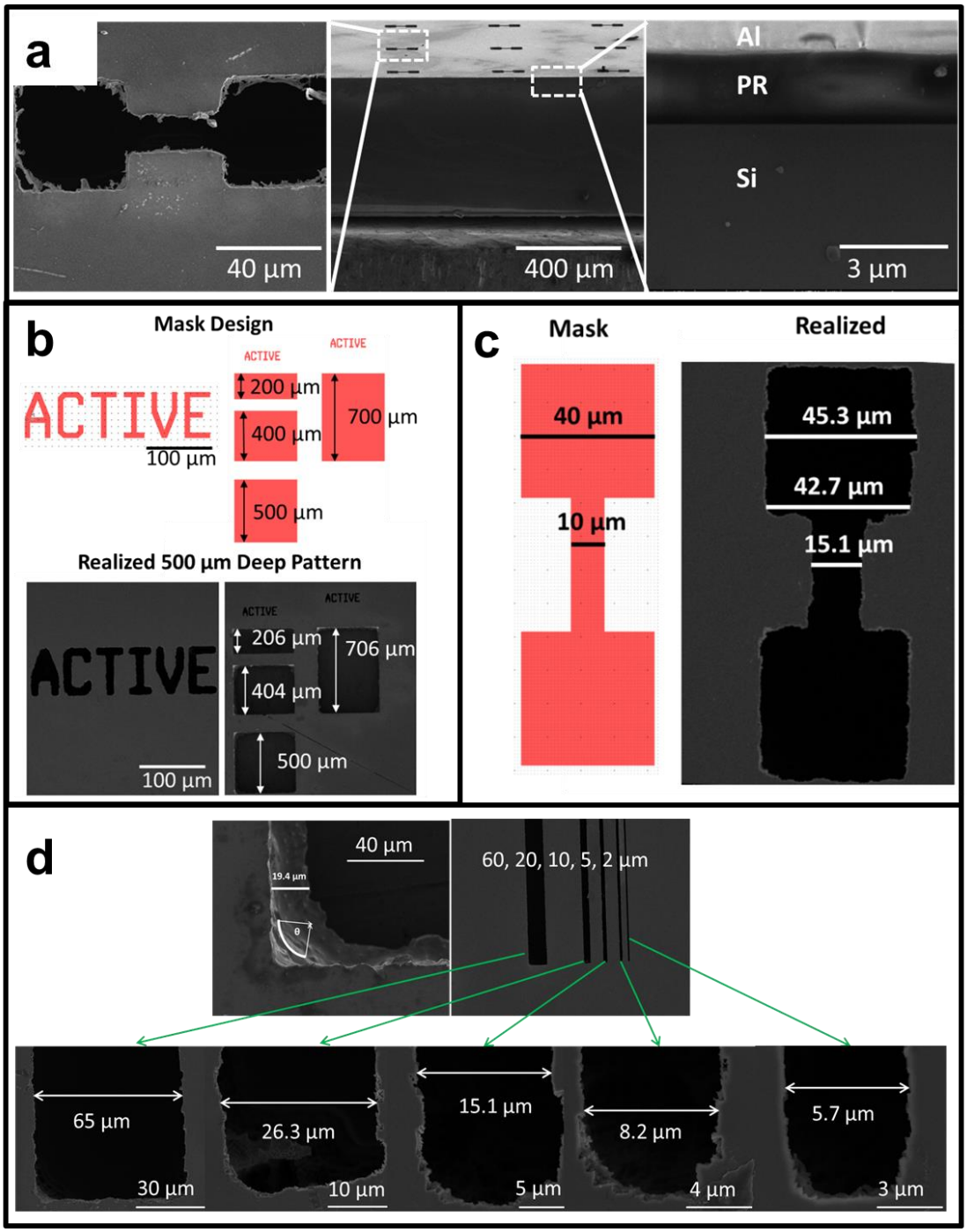

Figure 3. SEM images showing top view of patterned 500 µm features and cross sectional SEM showing the Si/PR/Al stack: (a) designed *vs.* realized deep features, (b) designed and realized fine features show that the distortion is almost constant, independent of feature size, (c) and (d) zoomed in SEM images for fine few microns features and edges.

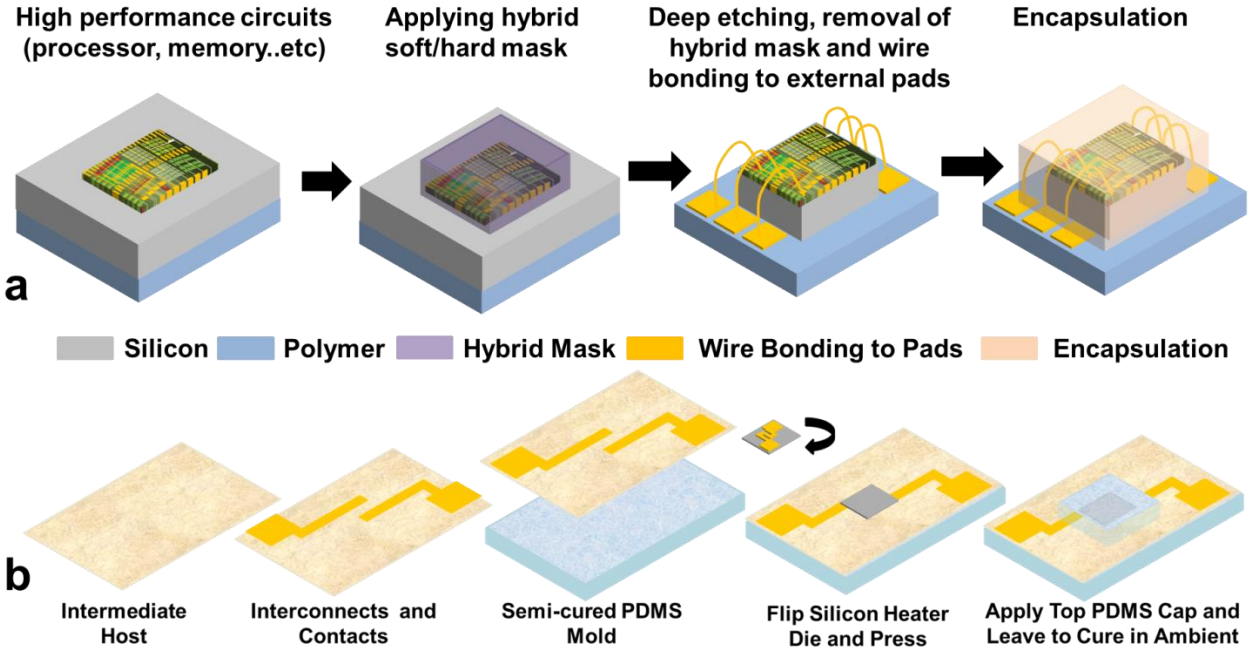

Figure 4. (a) Conceptual design of flexible packaging of high performance electronics using hybrid soft/hard mask etching technique, (b) utilized flow for packaging sample die in PDMS.

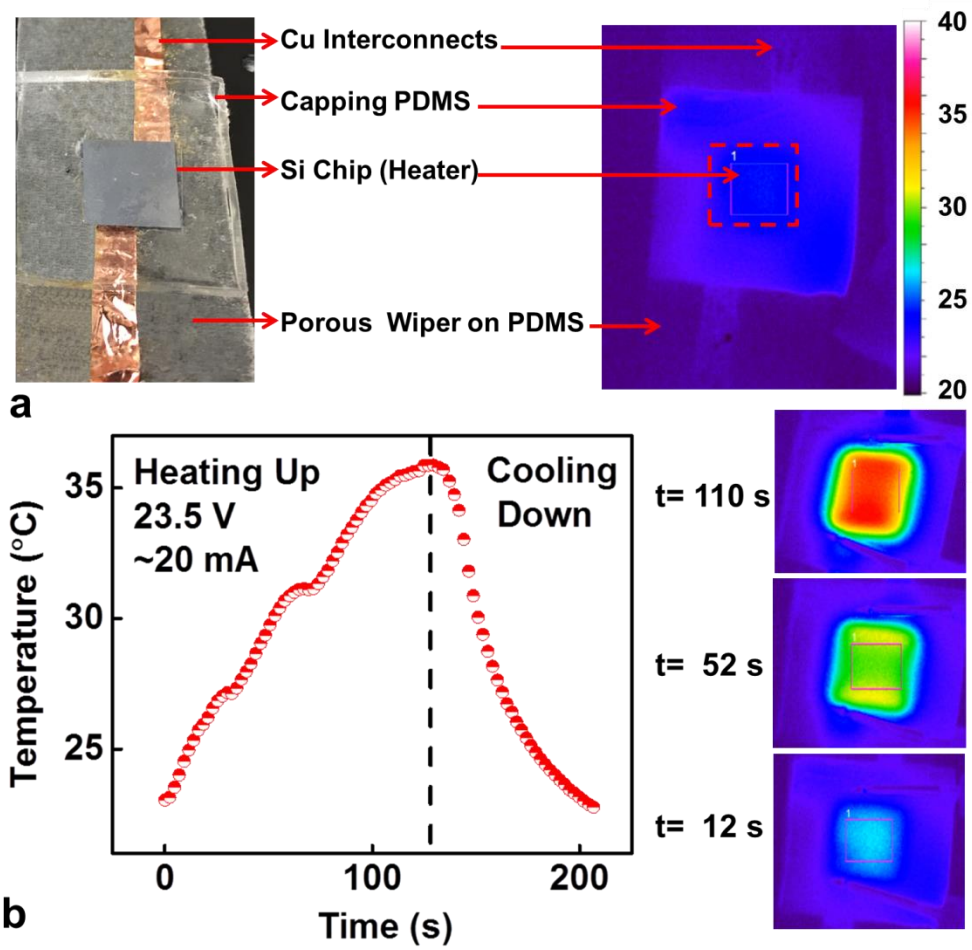

Figure 5. (a) Implementation of Figure 4b flow and (b) demonstrations of established contacts through heating up the encapsulated silicon heater chip.

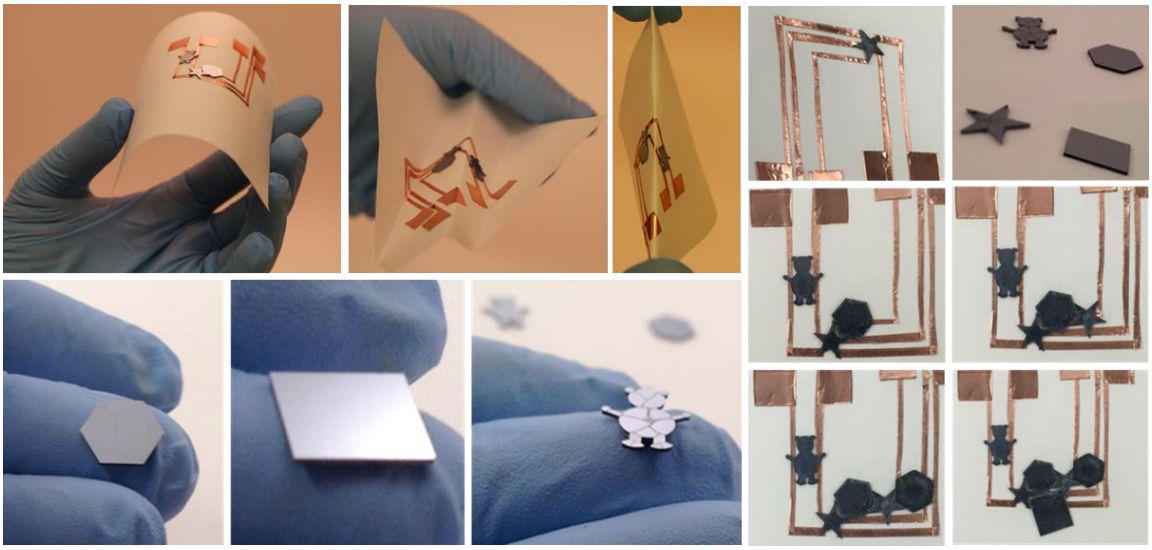

Figure 6. Diced asymmetric patterns using hybrid soft/hard mask for deep etching. The cracks around sharp angles are subject of further optimizations and they should not affect the devices on the other side. Top left images show the Lego dies on flexible substrate with interconnects. Side images show connection strategy and Lego concept for fitting dies on underlying interconnects.

Table 1. Summary of key deep etching works over the past few decades.

Ref.	Etching Technique	Maximum Depth (μm)	Aspect Ratio	Minimum Realized Feature (μm)	Year
[1]	SCREAM I (with self-aligned-metallization)	20	10	5	1994
[7]	Multilayer Ni/Al mask	200	10	20	1995
[4]	Black silicon method	200	10	20	1995
[6]	Silicon fusion bonding and DRIE	200	20	10	1996
[30]	Etch-diffusion process	40	20	2	1996
[31]	SiO_2 mask and high density plasma using SF_6/O_2 gases	100	50	1.2	1999
[32]	Time multiplexed deep etching (TMDE)	~500	~25	20	2001
[3]	Bosch process	40.1	107	0.374	2005
This work	Hybrid soft (PR)/hard(Al) mask	~500	~100	5	2016

A highly manufacturable deep reactive ion etching based process involving a hybrid soft/hard mask process technology shows high aspect ratio complex geometry Lego like silicon electronics formation enabling free-form (physically flexible, stretchable and reconfigurable) electronic systems.

Keyword: Lego, silicon electronics, deep reactive ion etching, soft/hard mask.

M. T. Ghoneim, M. M. Hussain*

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