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Experimental Behavior Evaluation of Series and Parallel Connected Constant Phase Elements

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Abstract

Fractional-order capacitors are the core building blocks for implementing fractional-order circuits. Due to the absence of their commercial availability, they can be approximated through appropriately configured passive or active integer-order element topologies. Such a topology, constructed using Operational Transconductance Amplifiers (OTAs) and capacitors has been implemented in monolithic form through the AMS 0.35 μ m CMOS process, and the fabricated chips are employed here for the experimental evaluation of the behavior of networks constructed from fractional-order capacitors connected in series or in parallel.

Key Words: Fractional-order circuits; fractional-order impedance; fractional-order capacitor; constant-phase element; fractional-order element emulator.

I. Introduction

Fractional-order circuit design has witnessed a rapid progress during the past few years both from circuit theoretic and implementation point of views due to its significant importance across several scientific disciplines [1]. At the heart of fractional-order circuit design are the generalized forms of capacitors and inductors known as fractional-order capacitors and inductors [2]-[3]. In particular, the impedance of a fractional-order capacitor, which is also known as constant phase element (CPE) [4], is described by

$$Z(s) = \frac{1}{C_a s^a} \quad (1)$$

The variable a ($0 < a < 1$) is the order of the CPE and is known as the dispersion coefficient, while C_a is a pseudo-capacitance expressed in $\text{Farad} \cdot \text{sec}^{a-1}$ ($\text{F} \cdot \text{sec}^{a-1}$). Thus, the value of the conventional capacitance (C) of a CPE, in Farad, can be calculated using the formula

$$C = \frac{C_a}{\omega^{1-a}} \quad (2)$$

which indicates that the capacitance of a CPE is a variable dependent on both frequency and order. However, the phase (θ) of this element is equal to $-\pi/2$ and is constant.

Although CPEs are not commercially, they have been realized in different ways; for example through the utilization of electrolytic processes, fractal structures on silicon, dipping capacitive type polymer-coated probes in a polarizable medium and, most recently, using graphene [4]-[6]. In addition, CPEs could be approximated around a center frequency ω_0 by appropriately configured integer-order RC networks, but this procedure is not easy from the design flexibility point of view, in the sense that tuning the order and/or pseudo-capacitance requires changing all circuit component values [7]-[11]. Recently, a discrete component realization of an active CPE emulator was presented

in [12], while an integrated version using OTAs as active elements was introduced in [13,14].

The main contribution of this work is that, according to the authors' best knowledge, this is the first time in the literature where the behavior of series and parallel connections of CPEs is experimentally evaluated. The content is organized as follows: the theoretical background is given in Section II, while in Section III the behavior of networks formed by CPEs in series or parallel connection, or a combination of both is experimentally verified using the chip fabricated and described in [13,14]. In [13] we validated experimentally the operation of individual CPEs but did not consider the case of series/parallel combinations of these elements, which is commonly done in their integer-order counter parts, i.e. ideal capacitors. As CPEs are important in fractional-order modeling of real-life systems, the work presented here aids in verifying the possibility of representing multiple parts of a complex system via CPEs of different orders and different pseudo-capacitances which can then be combined together to simplify the overall system model [15]. The behavior of the series and parallel connected CPEs at process, power supply voltage, and temperature (PVT) corners is evaluated in Section IV.

II. Series and parallel connection of CPEs

A. Series connection of CPEs

Let us consider the case that two CPEs with orders a_1 and a_2 , and pseudo-capacitances C_{a_1} and C_{a_2} , are connected in series as shown in Fig. 1.

Figure 1: Series connection of two fractional-order capacitors (CPEs).

Using (1), the equivalent impedance of this network ($Z_{eq,s}$) is expressed by (3)

$$Z_{eq,s} = \frac{\frac{1}{C_{a2}} s^{a_1} + \frac{1}{C_{a1}} s^{a_2}}{s^{a_1+a_2}} \quad (3)$$

Setting $s = (j\omega)^a = \omega^a [\cos(a\pi/2) + j\sin(a\pi/2)]$ [2], the magnitude of this impedance will be given by

$$|Z_{eq,s}| = \frac{\sqrt{\frac{1}{C_{a1}^2} \omega^{2a_2} + \frac{2}{C_{a1} C_{a2}} \omega^{a_1+a_2} \cos\left[\frac{(a_2 - a_1)\pi}{2}\right] + \frac{1}{C_{a2}^2} \omega^{2a_1}}}{\omega^{a_1+a_2}} \quad (4)$$

and its phase by

$$\arg(Z_{eq,s}) = \tan^{-1} \left(\frac{\frac{1}{C_{a2}} \omega^{a_1} \sin\left(\frac{a_1\pi}{2}\right) + \frac{1}{C_{a1}} \omega^{a_2} \sin\left(\frac{a_2\pi}{2}\right)}{\frac{1}{C_{a2}} \omega^{a_1} \cos\left(\frac{a_1\pi}{2}\right) + \frac{1}{C_{a1}} \omega^{a_2} \cos\left(\frac{a_2\pi}{2}\right)} \right) - \frac{(a_1 + a_2)\pi}{2} \quad (5)$$

Inspecting (5) it is obvious that the phase of this network is frequency dependent and not constant as for the individual CPEs. Consequently, its equivalent order ($a_{eq,s}$) is also frequency dependent and given as

$$a_{eq,s} = -\frac{\arg(Z_{eq,s})}{\frac{\pi}{2}} \quad (6)$$

This situation is not practical since the purpose of combining CPEs in series or in parallel is to obtain an equivalent CPE. However, with the equivalent order being frequency dependent, this target cannot be achieved. Therefore we consider identical CPEs which have the same pseudo-capacitances $C_{a_1} = C_{a_2} = C_a$ as well as the same order $a_1 = a_2 = a$, then, using (3), the expression for the total impedance simplifies to

$$Z_{eq,s} = \frac{1}{\frac{C_a}{2} s^a} \quad (7)$$

According to (7), the pseudo-capacitance is halved compared to that of a single CPE, while the equivalent order remains the same independent of frequency. This means that fractional-order capacitors follow the same rule as integer-order ones when combined in series only if they have both identical pseudo-capacitances and equal orders.

Generalizing for an n -series connection of CPEs with pseudo-capacitances C_{a_i} and order a_i ($i=1, 2, \dots, n$) results into a element with impedance described by (8)

$$Z_{eq,s} = \frac{C_{a_1}s^{a_1} + C_{a_2}s^{a_2} + \dots + C_{a_n}s^{a_n}}{C_{a_1} \cdot C_{a_2} \dots \cdot C_{a_n}s^{a_1+a_2+\dots+a_n}} \quad (8)$$

In the special case of identical CPEs, the series connection results in a CPE with pseudo-capacitance equal to C_a/n and equivalent (a) constant over the whole frequency range and equal to the order of the individual CPE. Thus, the total impedance for this case can be written as

$$Z_{eq,s} = \frac{1}{\frac{C_a}{n}s^a} \quad (9)$$

B. Parallel connection of CPEs

In the case of parallel connection of two CPEs with orders a_1 and a_2 , and pseudo-capacitances C_{a_1} and C_{a_2} , as shown in Fig. 2, the total impedance is simply

Figure 2: Parallel connection of two CPEs.

$$Z_{eq,p} = \frac{1}{C_{a_1}s^{a_1} + C_{a_2}s^{a_2}} \quad (10)$$

According to (10), the magnitude and phase responses of this equivalent impedance are respectively given by (11) and (12) as

$$|Z_{eq,p}| = \frac{1}{\sqrt{C_{a_1}^2 \omega^{2a_1} + 2C_{a_1} C_{a_2} \omega^{a_1+a_2} \cos\left[\frac{(a_1-a_2)\pi}{2}\right] + C_{a_2}^2 \omega^{2a_2}}} \quad (11)$$

and

$$\arg(Z_{eq,p}) = \tan^{-1} \left(\frac{C_{a_1} \omega^{a_1} \sin\left(\frac{a_1\pi}{2}\right) + C_{a_2} \omega^{a_2} \sin\left(\frac{a_2\pi}{2}\right)}{C_{a_1} \omega^{a_1} \cos\left(\frac{a_1\pi}{2}\right) + C_{a_2} \omega^{a_2} \cos\left(\frac{a_2\pi}{2}\right)} \right) \quad (12)$$

As in the case of the series connection, the equivalent fractional-order of the resulting network is frequency dependent and is given by the expression in (6). However, it can similarly be shown that for n identical CPEs connected in parallel, the equivalent impedance simplifies to

$$Z_{eq,p} = \frac{1}{nC_a s^a} \quad (13)$$

In other words, the equivalent element has a pseudo-capacitance equal to nC_a , while its equivalent order (a) is the same as that of the individual CPE meaning that only for the case of identical CPEs it is possible to obtain an equivalent CPE with constant phase.

C. Interconnection of series and parallel CPE networks

Let us now consider the network demonstrated in Fig. 3a. The equivalent impedance is given by the following expression

$$Z_{eq} = \frac{C_{a_1} C_{a_3} s^{a_1+a_3} + C_{a_1} C_{a_4} s^{a_1+a_4} + C_{a_2} C_{a_3} s^{a_2+a_3} + C_{a_2} C_{a_4} s^{a_2+a_4} + C_{a_1} C_{a_2} s^{a_1+a_2}}{C_{a_1} C_{a_2} C_{a_3} s^{a_1+a_2+a_3} + C_{a_1} C_{a_2} C_{a_4} s^{a_1+a_2+a_4}} \quad (14)$$

In the case of identical CPEs, the expression in (14) becomes

$$Z_{eq} = \frac{5}{2} \frac{1}{C_a s^a} \quad (15)$$

According to (15), the equivalent element has a pseudo-capacitance equal to $(2/5) \cdot C_a$, while its order (a) is the same as that of the individual CPEs forming the network.

(a)

(b)

Figure 3: Interconnection of series and parallel CPE networks (a) series, and (b) parallel.

Meanwhile, the total impedance for the network in Fig. 3b, is given by the expression in (16)

$$Z_{eq} = \frac{C_{a1} s^{a_1} + C_{a2} s^{a_2}}{C_{a1} C_{a3} s^{a_1+a_3} + C_{a1} C_{a4} s^{a_1+a_4} + C_{a2} C_{a3} s^{a_2+a_3} + C_{a2} C_{a4} s^{a_2+a_4} + C_{a1} C_{a2} s^{a_1+a_2}} \quad (16)$$

Considering identical CPEs, then it is readily obtained that

$$Z_{eq} = \frac{2}{5} \frac{1}{C_a s^a} \quad (17)$$

The expression in (17) indicates that the equivalent element has a pseudo-capacitance equal to $(5/2)C_a$, while the order (a) is the same as that of the individual CPE.

In the following section, we seek to provide experimental verification for the above findings.

III. Experimental results

A. Design Background

We recall here some relevant background related to the circuit that shall be used for experimental verification [14]. In particular, the emulation of CPEs around a center frequency ω_o is performed through the functional block diagram shown in Fig. 4, which is constructed from a fractional-order differentiator $H(s)=(\tau s)^a$, with $\tau=1/\omega_o$, and a voltage-to-current (V/I) converter that could be implemented by an appropriately configured Operational Transconductance Amplifier (OTA) with transconductance g_{mVI} .

Figure 4: Functional Block Diagram for CPE emulation.

The emulated impedance is given by the formula:

$$Z = \frac{1}{g_{mVI}(\tau s)^a} \quad (18)$$

According to (18) the realized impedance at $\omega=\omega_o$ is equal to $1/g_{mVI}$; in other words, it is determined by the transconductance of the V/I stage. Comparing (1) and (18) it is seen that the realized value of pseudo-capacitance is

$$C_\alpha = \frac{g_{mVI}}{\omega_o^a} \quad (19)$$

The approximation of the differentiator is performed through the employment of a second-order approximation such that

$$Z_{eq} = \frac{1}{g_{mVI}} \cdot \frac{G_2 s^2 + \frac{G_1}{\tau_1} s + \frac{G_o}{\tau_1 \tau_2}}{s^2 + \frac{1}{\tau_1} s + \frac{1}{\tau_1 \tau_2}} \quad (20)$$

where the relevant coefficients of (20) are summarized in Table 1.

Table 1: Design equations for the CPE emulator in Fig.5a.

τ_1	τ_2	G_2	G_1	G_o
$\tau \cdot \left(\frac{a^2 - 3a + 2}{-2a^2 + 8} \right)$	$\tau \cdot \left(\frac{-2a^2 + 8}{a^2 + 3a + 2} \right)$	$\frac{a^2 + 3a + 2}{a^2 - 3a + 2}$	1	$\frac{a^2 - 3a + 2}{a^2 + 3a + 2}$

The complete CPE circuit is shown in Fig. 5a with the employed OTA shown in Fig.5b where the MOS transistors are biased in the subthreshold region and hence the OTA transconductance is given by (21)

$$g_m = \frac{5 I_{bias}}{9 n V_T} \quad (21)$$

with I_{bias} being the external bias current, n being the subthreshold slope factor of a MOS transistor and V_T the thermal voltage (26mV@ 27°C). Due to the existence of V_T , the design is sensitive to the temperature variations and this will be investigated in Section 4. Details of transistor aspect ratios were given in [14].

(a)

B. Setup

In our design, a single external bias current (I_o) is required and a precision Keithley DC current source (model 6220) was used to generate this bias current. Note that internally, this current is equal to the bias current of the V/I converter stage as well as equal to I_{o2} (see Fig.5a) while the bias currents I_{o1} and the scaled versions $G_i I_{o1}$, ($i=0, 1, 2$ and $j=1, 2$) are implemented on chip by appropriately configured current-mirror stages.

Figure 6: Fabricated CPE emulator chip (a) die photo and (b) pin list.

The center frequency around which the emulated CPEs are tested is set by two external capacitors (see Fig. 6b) with the same value ($C_{ext} \equiv C_{1ext} = C_{2ext}$) according to the expression in (22), which is derived from the design equations in Table 1

$$\omega_o = \frac{5I_o}{9nV_T C_{ext}} \frac{8 - 2a^2}{a^2 + 3a + 2} \quad (22)$$

Using a bias current equal to $I_o = 95\text{nA}$ and suitable values of C_{ext} to set the center

frequency around $f_0=500\text{Hz}$, impedance was measured using a precision LCR meter with 100mV applied voltage. The following measurements were performed.

C. Measurements

First, we measured the magnitude and phase response of the equivalent impedance $Z_{eq,s}$ in the case of serial connection of identical CPEs was performed and the results are plotted in Figs. 7(a,b) along with the best linear fit of the data. Table 2 is a summary of the extracted values from these two Figures compared to the expected values given between parentheses. The very good agreement with the theory is clear both in magnitude and phase. Note that the natural logarithm is used in the plots of Fig. 7 and that the slopes of the best fit straight lines yield the equivalent order of the equivalent impedances.

Next, measurements were repeated for the case of parallel connected CPEs as given in the plots of Figs. 8(a,b) and, also, in Table 3. The best linear fittings are also plotted inside the figures showing very good agreement with the expected results.

Table 2: Performance characteristics of the serial connection of CPEs. The equivalent order is measured from the slope of the fitted magnitude response of Fig. 7a.

Connection	0.2+0.2	0.4+0.4	0.5+0.5	0.7+0.7	0.8+0.8
Phase @ ω_0	-16.9 (-18)	-35.9 (-36)	-43.1 (-45)	-60.6 (-63)	-70.9 (-72)
Order a	0.23 (0.2)	0.417 (0.4)	0.566 (0.5)	0.746 (0.7)	0.843 (0.8)

Table 3: Performance characteristics of the parallel connection of CPEs. The order is measured from the slope of the fitted magnitude response of Fig. 8a.

Connection	0.4//0.4	0.5//0.5	0.6//0.6	0.7//0.7	0.8//0.8
Phase @ ω_0	-37 (-36)	-43.7 (-45)	-53.5 (-54)	-61.2 (-63)	-71.7 (-72)
Order a	0.45 (0.4)	0.57 (0.5)	0.65 (0.6)	0.75 (0.7)	0.84 (0.8)

Inspecting the results in Tables 2-3, it is concluded that the series and parallel connections of identical CPEs is in agreement with (9) and (13). As a final confirmation, Fig. 9 shows a comparison of the magnitude and phase of 2 CPEs of order 0.5 connected in series and in parallel, compared to a single CPE. It is clear that the phase remains identical and so does the order of the combination with the only change being in the impedance magnitude reflecting the change in C_a which is measured as $92.13\text{nF sec}^{-0.5}$ for the parallel connection, $25.11\text{nF sec}^{-0.5}$ for the series connection and $50.7\text{nF sec}^{-0.5}$ for the individual device.

(a)

(b)

Figure 7: Experimental results of the series connection of two CPEs of identical order and best fitting **(a)** magnitude, and **(b)** phase.

(a)

(b)

Figure 8: Experimental results of the parallel connection of two identical order CPEs and best fitting a) magnitude, and b) phase.

Figure 9: *Experimental results of the parallel and series connections of two identical 0.5 order CPEs compared to single CPE both in magnitude and phase.*

According to (22) the center frequency, around which that the emulation of CPEs is performed, can be tuned through the external capacitors. The tuned elements have been tested in the case of the networks shown in Fig. 3, considering identical CPEs of order 0.5 and $f_o=100\text{Hz}$. The experimental magnitude and phase responses of impedance, are shown in Figs. 10(a,b) along with the best linear fit of the data. From these plots, it is readily concluded that the order as well as the phase are very close to those theoretically predicted for both networks. Also, the time-domain behavior of these networks has been experimentally evaluated at 50Hz with a 100mV_{pp} sinusoidal voltage. The voltage and current waveforms are plotted in Figs. 11(a, b), respectively for the two networks of Fig. 3. The measured phase difference is equal to -41° , which is close to theoretically predicted value of -45° .

(a)

(b)

Figure 10: Experimental results of the networks in Fig. 3 using identical order CPEs and best fitting (a) magnitude, and (b) phase.

(a)

(b)

Figure 11: Experimental time-domain voltage-current waveforms at 50Hz for the networks in (a)

Fig. 3a and (b) Fig.3b.

IV. Corner analysis

The behavior of the series and parallel connected CPEs at process, power supply voltage, and temperature (PVT) corners has been evaluated over 16 different PVT corners. Thus, worst case power (fast-fast), worst case speed (slow-slow), worst case one

(fast-slow), and worst zero (slow-fast) {wp, ws, wo, wz} MOS transistors model parameters, {0°C, 27°C, 60°C} temperature values, and $\pm 5\%$ supply voltages variations have been considered. The Analog Design Environment of the Cadence suite was used. In the case of a series connection of CPEs of order 0.5, the magnitude and phase plots are depicted in Fig.12.

(a)

(b)

Figure 12: PVT corner analysis results for the series connection of two identical CPEs of order 0.5 (a) magnitude and (b) phase.

(a)

(b)

Figure 13: *PVT corner analysis results for the parallel connection of two identical CPEs of order 0.5 (a) magnitude and (b) phase.*

The obtained corners of the magnitude are $1.13\text{M}\Omega$ and $1.37\text{M}\Omega$, while the nominal value was $1.28\text{M}\Omega$. The corresponding corners of phase at 100Hz were -47.2° and -43.7° , with the corresponding nominal value being equal to -45° . The PVT corner analysis results for the parallel-connected CPEs of order 0.5 are also depicted in Fig.13. The obtained corners of the impedance magnitude are $283\text{k}\Omega$ and $343\text{k}\Omega$, while the nominal value was $320\text{k}\Omega$. The corresponding corners of phase at 100Hz were -47.2° and -43.9° , while nominal value is -45° .

V. Conclusion

Experimental results confirming the predicted behavior of series and parallel connections of identical fractional-order capacitors were presented for first time in the literature. The platforms for the experiments were two fabricated chips containing a variety of CPEs with different orders. Of course, it is possible to combine in series or parallel CPEs of arbitrary orders, but the resultant impedance can be termed as a CPE only if the combined CPEs have identical orders. For that purpose, experimental results shown here have focused on all possible combinations of CPEs of identical orders from 0.2 up to order 0.8, as realized on the purpose-built chips. The ability to fabricate CMOS-based CPE emulators accurate over a wider frequency range is related to replacing the second-order approximation in (20) with a higher-order approximation and can be achieved relatively easy but on the expense of a more complex circuitry. However, for many applications such as fractional-order controller design, the second-order approximation (accurate over 2 decades) is sufficient [16], [17].

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