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Highlights

- A 4-bit parity checker circuit is proposed and demonstrated based on recently developed microelectromechanical systems (MEMS) resonator based logic elements.
- Multiple copies of MEMS resonator based *XOR* logic gates are used to construct a complex logic circuit.
- This work demonstrates the functionality and feasibility of microresonator based logic platform for implementation of energy efficient complex digital circuits.

A Parity Checker Circuit Based on Microelectromechanical Resonator Logic Elements

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Abstract— Micro/nano-electromechanical resonator based logic computation has attracted significant attention in recent years due to its dynamic mode of operation, ultra-low power consumption, and potential for reprogrammable and reversible computing. Here we demonstrate a 4-bit parity checker circuit by utilizing recently developed logic gates based on MEMS resonators. Toward this, resonance frequencies of shallow arch shaped micro resonators are electrothermally tuned by the logic inputs to constitute the required logic gates for the proposed parity checker circuit. This study demonstrates that by utilizing MEMS resonator based logic elements, complex digital circuits can be realized.

I. INTRODUCTION

Electromechanical computing has attracted significant attention in the past decade driven by the need to replace transistors, as their miniaturization is approaching the physical limits and their energy efficiency is degrading, by smarter multi-function logic elements [1]. With the fabrication capabilities reaching molecular level [2], the notion of mechanical computing has been revitalized and revamped. MEMS/NEMS static switching devices capable of performing multiple logic operations have been demonstrated in the past few years [3-8]. Despite some major advantages, such as cascadeability and ideal leakage properties, these devices have some significant limitations due to contact reliability, contact resistance, surface forces and mechanical delay. To overcome

these drawbacks, researchers have been exploring dynamic MEMS/NEMS devices such as micro resonators as logic elements [9-20], despite their limitations in terms of speed of operation and complexity in building combinational logic circuits. Although there have been successful demonstrations of memory components [9-11], 2-bit logic gates [12-14] and multi-bit logic circuits [14], the realization of complex combinational logics has remained a challenge.

The first demonstration of a dynamic logic, based on a linear NEMS resonator gate, was presented in [12]. The high (low) amplitude response of the resonator at on-resonance (off-resonance) state was defined as the logic output 1 (0). Later, a nonlinear NEMS resonator was used to realize a noise assisted and reprogrammable 2-bit logic device [13]. Mahboob et al. [14] utilized parametric excitation scheme on a single micromechanical resonator to realize a multifunctional logic element to demonstrate 2-bit and multibit complex logic operations. Also, several components of a microcomputer, namely, byte memory, shift-register, and a controlled-NOT gate have been realized in [15] based on the higher order modes of parametrically excited NEMS resonator. Using four coupled, linearly operating nano-resonators, a reversible logic gate, Fredkin gate, has been realized for the first time [18]. Both physical and logical reversibility has been successfully demonstrated. Recently, we have proposed and demonstrated a logic element based on electrothermal resonance frequency tuning of a linearly operated MEMS arch shaped clamped-clamped beam resonator [19]. Although, we have shown all the fundamental 2-bit and basic n-bit logic operations, feasibility of building more complex logic circuits based on multiple copies of these logic gates has not been investigated.

The logic parity checker is an essential component for computing systems and information processing chips, in which the accurate matching of all transmitted and received data needs to be verified. To date no attempt has been made to realize this important logic component in the

micro/nano-resonator based logic platform. The proposed 4-bit parity checker circuit in this work consists of two *XOR* gates, similar to that proposed in [19], and a differential amplifier to combine the logic outputs of the two *XOR* gates to constitute the final logic output. The parity of the number of logic 1s among the 4 logic inputs is determined and the output signal gives logic state 0 for even parity and 1 for odd parity.

II. IMPLEMENTATION AND RESULTS

Fig. 1(a) and (b) shows a schematic and the SEM image of the fabricated device, respectively. The devices are fabricated on a highly conductive silicon device layer of a silicon on insulator (SOI) wafer by two-mask process [19]. Each device consists of a resonating microbeam and drive and sense electrodes to facilitate electrostatic actuation and capacitive detection. The dimensions of the arch beams are: $L = 500\mu\text{m}$, $W = 3\mu\text{m}$, $H = 30\mu\text{m}$. The gap between the actuating electrode and the microbeam is $G_0 = 8\mu\text{m}$, at the clamped ends and $G = 11\mu\text{m}$, at the mid-point due to $3\mu\text{m}$ of initial curvature, which is defined by the photo-lithography process to deliberately produce an in-plane arch microbeam.

(a)

(b)

Fig. 1. (a) Schematic of the microbeam resonator, (b) The SEM image of a fabricated device.

Fig. 2(a) shows a standard 4-bit parity checker logic block implemented with three *XOR* gates. Fig. 2(b) shows the schematic of the proposed micro resonator based parity checker circuit. The AC input signal is constantly applied at a fixed frequency and depending on the logic inputs, the logic output, V_{OUT} , is measured across the load resistor, R_L . Note that a high amplitude of V_{OUT} is measured due to a resonance signal, which is defined as the logic output 1(0).

Fig. 2. (a) Schematic of a standard parity checker logic circuit utilizing *XOR* gates. (b) Schematic of the proposed parity checker circuit utilizing microresonator based *XOR* gates. V_{OUT} represents the logic output where a high (low) amplitude corresponds to logic output state 1(0).

Fig. 3 shows the experimental setup. Res. *X* and Res. *Y* are biased with a single DC source, $V_{DC} = 50V$. The driving electrodes of the two micro resonators are provided with the same AC drive signal from the output port of the network analyzer (Agilent E5071C). Res. *X* output produces $A \oplus B$ logic output whereas Res. *Y* output produces $C \oplus D$ logic output. The two output signals are subsequently connected to a low noise amplifier (LNA) working in the differential amplifier mode to add and amplify the AC signal. This low noise amplifier (LNA), in its differential amplifier mode, effectively constitutes the third *XOR* gate necessary to complete the logic operation for the

proposed parity checker circuit. The final output of the proposed circuit is $P = (A \oplus B) \oplus (C \oplus D)$, which is same as that of a conventional parity checker circuit shown in Fig. 2 (a).

Fig. 3. Experimental setup of the microresonator based 4-bit parity checker circuit. A , B , C , and D logic inputs are represented as switches. Switch ON (OFF) corresponds to logic input 1 (0). Res. X produces $A \oplus B$ and Res. Y produces $C \oplus D$ at the corresponding sense electrodes. Finally, both signals are differentially added by the differential amplifier, which works as the third XOR gate to produce the final logic output $P = (A \oplus B) \oplus (C \oplus D)$.

The four logic inputs are provided with four different DC voltage sources, V_A , V_B , V_C and V_D , which are connected across the microbeams with series resistors, R_A , R_B , R_C , and R_D , and switches, A , B , C , and D , respectively, as shown in Fig. 3. The logic input 1(0) is defined by connecting (disconnecting) V_A , V_B , V_C , and V_D from the electrical network by the four switches, A , B , C , and D , respectively. So logic input 1(0) is represented by the switch ON (OFF) condition for switches A , B , C , and D . The sensing electrodes are used to obtain the output signals from Res. X and Res. Y , which perform $A \oplus B$ and $C \oplus D$ logic operations, respectively. Finally, both of the output signals are differentially added using the LNA to produce the final logic output, P . Note that a high (low) S_{21} transmission signal corresponds to the logic output 1(0).

We use two similar arch micro resonators, Res. X and Res. Y with resonance frequencies around 120.95 kHz and 122.42 kHz, respectively. The Res. X and Res. Y microbeams show 110 Ω and 118 Ω resistance, respectively. Note that the difference in the resonance frequencies is due to

the fabrication variations in the wafer, and does not adversely affect the functionality of the logic block. All the experiments have been conducted at ~ 2 Torr pressure and at room temperature. Fig. 4 shows experimentally obtained frequency response of Res. X driven by an AC signal of 0.022V. The resonance frequency of the micro resonator is around 120.95 kHz with a quality factor around 528.

Fig. 4. Frequency response of a micro resonator (Res. X).

Fig. 5. Electrical circuit configurations for A and B logic inputs. (a) For (0 0) logic condition the total current flowing through the microbeam R_{MB} is, $I_{Tl} = 0$. (b) For (0 1), switch A is OFF and switch B is ON, hence, the total current is, $I_{Tl} = I_B$. (c) For (1 0), switch A is ON and switch B is OFF, hence, the total current is, $I_{Tl} = I_A$. (d) For (1 1), both the switches, A and B are ON, hence, the total current is $I_{Tl} = I_A + I_B > I_A$ or I_B .

Fig. 5 shows electrical circuit configurations between node E and F of Fig. 3 for different combinations of A and B logic inputs. Fig. 6(a) shows frequency responses of Res. X for different combinations of logic inputs A and B . For logic input (0 0) condition, the total current flowing through Res. X microbeam is $I_{Tl} = 0$, Fig. 5(a). In this case, Res. X shows resonance at 120.95 kHz

with an AC actuation signal of 0.056V, Fig. 6(a). Note that we increased the AC actuation voltage to 0.056V from the initial actuation voltage of 0.022V (Fig. 4), to achieve better signal to noise ratio. For logic input (0 1) or (1 0) conditions for A and B , either V_B or V_A is connected to Res. X microbeam, as shown in Fig. 5(b) and Fig. 5(c), respectively. Hence, the total DC current flowing through the microbeam of Res. X is either $I_{TI} = I_B$ or $I_{TI} = I_A$. We chose $V_A = V_B = 0.4\text{V}$, and $R_A = R_B = 50\Omega$. These values satisfy the condition $I_A = I_B$, and the resulting current generates enough heat and causes thermal expansion while flowing through the microbeam that induces compressive axial force. Since the microbeam is clamped at both ends, its curvature increases which in turn increases its stiffness. Thus, for (0 1) or (1 0) logic inputs, the resonance frequency of Res. X increases to 125.4 kHz. Note here that the voltage values for V_A and V_B are chosen for a specific resonance frequency of operation, 125.4 kHz in this particular case, therefore, any values can be chosen as long as we fix the logic circuit operation frequency accordingly. Now for logic input (1 1), both of the voltage sources, V_A and V_B , are connected to the microbeam, as illustrated in Fig. 5(d). In this case, the total current $I_{TI} = I_A + I_B > I_A$ or I_B . Hence, the resonance frequency of Res. X increases further to around 127.3 kHz, Fig. 6(a). Similarly, frequency responses for different combinations of logic inputs C and D are shown in Fig. 6(b). For (0 0) condition for C and D logic inputs, Res. Y shows resonance frequency around 122.42 kHz, Fig. 6(b). For logic inputs C and D , the resonance frequency of Res. Y increases to 125.4 kHz for (1 0) or (0 1) logic input conditions, for $V_C = V_D = 0.3\text{V}$, and $R_C = R_D = 50\Omega$. And for logic input (1 1), both of the voltage sources, V_C and V_D , are connected to the microbeam, hence, the resonance frequency of Res. Y increases to 126.7 kHz, Fig. 6(b). It's important to note here that for (1 0) or (0 1) logic input conditions for A and B , and C and D , the resonance frequencies of Res. X and Res. Y coincides around 125.4 kHz. This is the designed AC signal frequency for the implementation of the proposed parity checker circuit.

Fig. 7(a) and (b) shows the frequency responses at the output port of the circuit with different logic input combinations. For logic input condition (0 0 0 0), the frequency response is plotted in black, Fig 7(a).

(a)

(b)

Fig. 6. (a) Frequency responses of Res. X for different logic input (A, B) conditions, (b) Frequency responses of Res. Y for different logic input (C, D) conditions.

Since both Res. X and Res. Y show off-resonance state at 125.4 kHz, which is the driving frequency of our circuit, the logic output in this case is 0. For the case of logic input condition (0 1 0 0), Res. Y is at off-resonance state at 125.4 kHz while Res. X is at on-resonance state, shown in blue in Fig. 7(a). The logic output in this case is 1. Now, for the case of logic input condition (0 1 0 1), both Res. X and Res. Y resonance frequencies coincide at 125.4 kHz. Since we are using differential amplifier configuration to add two signals coming from the microresonator outputs, the

final output signal is attenuated to low S_{21} transmission signal level at 125.4 kHz, as shown in Fig. 7(a) in orange. Note that since there is some mismatch with the frequency responses of the two micro resonators, a spike of high amplitude signal around 125.3 kHz is observed. However, since the AC input signal frequency for the proposed parity checker circuit is chosen to be 125.4 kHz, the output in this case will be a logic 0, as required for the successful operation of the parity checker circuit. Few other input combinations and corresponding frequency responses are shown in Fig. 7(a) and (b). Remaining logic input combinations and corresponding frequency responses can be similarly realized, which are not shown here for brevity. Finally, Fig. 8 shows the circuit operation at a fixed AC signal frequency of 125.4 kHz. Different combinations of 4-bit logic inputs and the corresponding logic outputs are plotted for 100 seconds. The proposed circuit indeed shows the correct parity output, where odd number of 1s produces logic output 1, as expected.

(a)

(b)

Fig. 7. (a) Frequency responses at the output of the parity checker circuit for 0000, 0100, 0101, 1011, and 1111 logic conditions. (b) Frequency responses for 1000, 0010, 0111, 0010, and 1010 logic conditions. The AC operating frequency is set at 125.4 kHz, which is shown as the dotted line in the figures. Also, the corresponding logic outputs, 1/0 are marked. Frequency responses for the remaining six input combinations are not shown here for brevity, which can be similarly realized.

Fig. 8. Demonstration of the parity checker circuit operation with a time sweep, where A , B , C , and D logic inputs are changed and the corresponding logic output is plotted. The frequency of the AC signal is chosen to be 125.4 kHz. The logic circuit produces correct output signal, where the odd number of 1s only produces logic output 1.

III. DISCUSSION

An accurate assessment of the merits of micro/nano-resonators based logic circuits, including the ones presented in this work, requires careful consideration of several technological issues. One of the concerns is regarding the required DC bias voltage for correct operation. This voltage can be reduced to an acceptable level ($\sim 5V$) by hermetically sealing the circuits at lower pressures and by scaling and shrinking the gap between the resonating beam and the drive/sense electrode. Another aspect is the energy consumption due to the structure activation by an AC signal provided to the driving electrode. Although not directly related to the logic operation, it contributed to the overall energy cost in the circuit. In this paper, we refer to this energy as the driving energy. The amount of energy consumed for the actual logic operations is related to the DC logic input signals, which is called the logic operation energy.

For the AC driving energy, it is estimated conservatively based on the method described in [12, 13], in a unity gain system:

$$I = \frac{10^{\frac{S_{21}}{20}} \cdot V}{R} \quad (1)$$

$$E_{Driving} = V \cdot I \cdot t_s \quad (2)$$

, where $V = 0.056V$, is the AC driving voltage, I is the RMS value of the AC current, $R = 50\Omega$ for unity gain, and $t_s = 0.7ms$, is the switching time of the resonator ($Q/2\pi f$) [9]. Thus, by calculating the AC current flowing in the circuit according to Equation (1) from the measured S_{21} results (-78dB), an AC driving energy of 5.54pJ per logic operation is estimated as per Equation (2).

For the logic operation in this circuit, the logic input voltage sources (V_A , V_B , V_C , and V_D) dominate the total energy consumption. Except one combination of the logic inputs ($A=B=C=D=0$), all the other combinations require DC current passing through the microbeams, as illustrated in Fig. 5 for Res. X . The logic operation cost for the circuit can be separated in two parts, Res. X for the logic inputs A and B , and Res. Y for the logic inputs C and D . Each resonator responds to 4 (2^2) different logic input combinations, thus the total input combinations for the parity checker circuit is 16 (2^4). Res. X and Res. Y essentially operates in an identical way when comes to four different input combinations, the only differences between these two resonators are the resistance of the microbeams (R_{MB}) and the logic input voltages. Therefore, here we illustrate all different combinations for the Res. X , and those for Res. Y can be obtained in a similar way. Note that t_s is the switching time of the resonator as mentioned before.

Case 0: $AB = (0\ 0)$

No DC current ($I_{TI} = 0$), the logic operation cost is 0.

Case 1: $AB = (1\ 0)$ or $(0\ 1)$

$$I_{T1} = I_{A(B)} = \frac{V_{A(B)}}{R_{A(B)} + R_{MB}} \quad (3)$$

$$E_{Logic/op} = I_{T1}^2 \cdot (R_{A(B)} + R_{MB}) \cdot t_s \quad (4)$$

Case 2: $AB = (1\ 1)$

$$I_{A(B)} = \frac{V_{A(B)}}{R_{A(B)} + 2R_{MB}}, \quad I_{T1} = I_A + I_B \quad (5)$$

$$E_{Logic/op} = (I_A^2 \cdot R_A + I_B^2 \cdot R_B + I_{T1}^2 \cdot R_{MB}) \cdot t_s \quad (6)$$

We estimated the energy cost per logic operation based on Equations (3) to (6), a similar method used in [19]. Equation 5 is obtained assuming $R_A \approx R_B$. The average energy consumed by the parity checker circuit is 1.25 μ J per logic operation.

For the given structure, the logic operation energy cost can be further reduced at least by an order of magnitude by selecting a narrow frequency range for successful operation of the device. For example, with similar resonators (Res. X and Res. Y), a frequency shift of only 1 kHz will suffice for the proper logic operation (distinct difference between logic output 0 and 1), instead of 4.5 kHz shift used for Res. X in this work. This will reduce the DC voltage load for the logic inputs to 0.1V [21]. Hence, an average energy cost per logic operation will be 0.1 μ J, a ten time reduction from the earlier estimation. With careful design (selecting narrow frequency window of operation) and device miniaturization, the required level of power consumption for switching operation is expected to decrease. Moreover, the switching time of the resonator would be much faster, at least in micro-seconds (for $Q \sim 1000, f \sim 400$ MHz), for the state-of-the-art technology [22]. Even with a conservative assumption that the scaled structure would have similar power consumption, when

device switching speed reaches the state-of-the-art technology, energy consumption per logic operation would decrease to 8% of the current value.

In order to drive another resonator logic block or to be used in other circuit applications, proper amplification of the output AC signal is crucial, which will contribute to the total energy consumption. For an amplification of 85dB [23], an increase of 1% of the total energy cost can be expected for the current test setup. For the microresonators used in this work, a maximum operation speed of 1.4 kHz can be achieved, which is defined by the resonator switching speed (ring down time) rather than the thermal switching speed (heating/cooling time) of the microbeam [19]. For the implementation using transistors, as per the simulation results, a parity checker circuit built in TSMC 65nm CMOS technology [24] consumes 0.13pJ per logic operation for the current operation frequency. The main reason for the large disparity between the resonator based circuit (1.25 μ J/operation) and the CMOS based circuit (0.13pJ/operation) is that the switching time of the resonator is much slower than that of a transistor. It's worth mentioning here that at the ultimate limit of scaling, a resonator switching time in tenth of nano-seconds can be envisioned for resonance frequency in GHz [25, 26]. This will ultimately reduce the energy per operation based on nano-resonator logic devices to a level that would be significantly lower than the CMOS counterparts.

IV. CONCLUSION

In this work we have proposed a MEMS resonator based parity checker circuit. The realization of such a key logic and information processing element, in addition to previously demonstrated core logic blocks, shows the potential of this technology as an appealing alternative for implementation of Very Large Scale Integrated (VLSI) circuits and the next generation of ultra-low power micro/nano-electromechanical computers. While this work demonstrates the functionality and feasibility of microresonator based logic platform, advanced scaling techniques

and full integration of microresonators could enable energy efficiency gains over current technologies.

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