CMOS technology: a critical enabler for free-form electronics-based killer applications

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ABSTRACT

Complementary metal oxide semiconductor (CMOS) technology offers batch manufacturability by ultra-large-scale-integration (ULSI) of high performance electronics with a performance/cost advantage and profound reliability. However, as of today their focus has been on rigid and bulky thin film based materials. Their applications have been limited to computation, communication, display and vehicular electronics. With the upcoming surge of Internet of Everything, we have critical opportunity to expand the world of electronics by bridging between CMOS technology and free form electronics which can be used as wearable, implantable and embedded form. The asymmetry of shape and softness of surface (skins) in natural living objects including human, other species, plants make them incompatible with the presently available uniformly shaped and rigidly structured today's CMOS electronics. But if we can break this barrier then we can use the physically free form electronics for applications like plant monitoring for expansion of agricultural productivity and quality, we can find monitoring and treatment focused consumer healthcare electronics – and many more creative applications. In our view, the fundamental challenge is to engage the mass users to materialize their creative ideas. Present form of electronics are too complex to understand, to work with and to use. By deploying game changing additive manufacturing, low-cost raw materials, transfer printing along with CMOS technology, we can potentially stick high quality CMOS electronics on any existing objects and embed such electronics into any future objects that will be made. The end goal is to make them smart to augment the quality of our life. We use a particular example on implantable electronics (brain machine interface) and its integration strategy enabled by CMOS device design and technology run path.

Keywords: CMOS, free form electronics, brain machine interface.

INTRODUCTION

According to the World Health Organization (WHO), nearly 20% of the world's population suffers from various neurological illnesses including but not limited to Alzheimer's Disease, multiple sclerosis, autism, dementia, paralysis, epilepsy, traumatic brain injury and such. Neuropsychiatric disorders are among the leading causes of worldwide disability in young people.¹ It is thus imperative to study and understand the neurological condition of our brain. According to US National Academy of Engineering, one of the grandest engineering challenges of the 21st century is development of high-resolution high-performance implantable electronics and their placement in the intracranial space and on the brain's soft tissue.² By gathering neurological signals generated in the brain, such systems can offer invaluable information. If we enhance the functionality of such systems for stimulation then they can provide critical clinical therapeutic to Parkinson's disease and other neurological disorders.^{3, 4} Still, a convenient mobile system for chronic use is yet to be developed that can monitor the neurological activities. We show a new way to develop a Brain Machine Interface (BMI) system that will be (i) implantable but non-penetrating, eliminating possibility of hemorrhage and inflammatory tissue responses; (ii) physically flexible to be compliant on asymmetric soft surfaces of the brain; (iii) ultra-dense high-performance, ultra-low-power CMOS electronics integrated for large area mapping and high-resolution data acquisition; (iv) fully implantable (wireless data transmission and power supply) and (v) for chronic use with ease (portable and no wire out after implant). Before discussing our proposed system and research methodology in detail, we first provide a brief status-quo survey on various methods available today for brain machine interfacing.

Historically, the field of neuroscience advanced through the groundbreaking discovery of functional magnetic resonance imaging (fMRI) which helped developing important understanding of the brain's activities.⁵ Similar advances in real-time monitoring of neuronal activity also happened through confocal microscopy and two photon techniques.^{6, 7} Next,

positron emission tomography yielded molecular level neuroimaging features.⁸ Additionally, development of optogenetics⁹, optically transparent molecular interrogation¹⁰, miniaturized fluorescence microscopy for cellular-level brain imaging in freely moving animals^{11, 12}, and transgenic strategies for neurons¹³ has advanced the field appreciably in the recent past. Although they are mostly non-invasive, these technologies are often too large and too heavy to be portable. Finally they are prohibitively expensive for wide deployment.

Electroencephalography (EEG) is a form of surface conformal neural interface systems.¹⁴⁻¹⁷ It is non-invasive. It applies arrays of electrodes over the scalp using conducting pastes or gels. Physically EEG is not feasible for long periods of operation as the gels or pastes dry out. Also the acquired signals are often of poor quality.

Penetrating through the skulls into the brain, micro-needle electrode arrays (popularly known as Utah arrays¹⁸) offer high-resolution interfacing to a small area of cortex and enable high-performance neuromotor prostheses¹⁹. But, they can function for a limited time (6–12 months²⁰) due to the diminishing signal quality on most electrodes, penetration related hemorrhage and inflammatory tissue responses from the immediate insertion area²¹⁻²³.

In contrast, highly flexible arrays of non-penetrating subdural electrodes in Electrocorticography (ECoG) have unique advantages due to their placement on the cortical surface. They maintain signal quality over extended periods of time with minimized irritation and injury to brain tissues²⁴⁻³⁴. Furthermore, the gathered information from the recorded signal are comparable to that of the penetrating microelectrodes³⁵⁻³⁷. Still massive wiring limits its spatial resolution to 196 electrodes in 12.3 mm² area³⁸. Integration of functionalities like wireless, remote power supply, massive parallelism, single-cell reading, longevity of electrodes are desired features for such system.

Therefore, in future, large-scale compliant BMI systems for chronic use with high temporal and spatial precision of recordings over large cortical surface are critical. A physically flexible fully wireless implantable integrated BMI system with all the required electronic components remains as an elusive goal. Specially, data management electronics are mainly silicon based complementary metal oxide semiconductor (CMOS) electronics due to their superior electron transport property, maturity in CMOS processing and reliability. Although organic/molecular electronics achieve unprecedented flexibility and low cost, and graphene or other two dimensional materials show higher mobility and flexibility – for wide deployment of BMI systems, silicon CMOS can play crucial role. They offer high-performance data processing, relatively low power operation and ultra-large-scale-integration (ULSI) density in a relatively cost-effective manner. However, they are bulky and rigid in their physical form. Commercially available ultra-thin silicon can be flexible but crystalline defects in such silicon are prohibitively high to achieve high-performance. Also, they are too lightweight and thin making them unusable for safe-handling and high thermal budget processing due to rapid physical deformation caused by residual stress build-up. Finally they are highly expensive. Buffered substrates like silicon-on-insulator (SOI) (including ultra-thin and extremely-thin: UT/ETSOI) can provide high quality sophisticated ultra-scaled electronics³⁹⁻⁴¹ by removing the buffer layer (most often buffer oxide) but they are far more expensive than that of bulk mono-crystalline silicon (100) which is used for 90% of the silicon electronics manufacturing. Alternate orientation silicon substrates can be used like Si (110) or Si (111)⁴². However, the former has lower electron mobility (whereas 65% of the transistors in a circuitry depend on high electron mobility) and the latter has more defects to yield comparable performance to that of a Si (100) substrate. Finally they are more expensive than that of traditional bulk Si (100) substrates. From a performance/cost perspective although bulk Si (100) offers great advantage, their <111> orientation vertical plane with the highest crystalline density makes it extremely difficult to be etched for their layered release from the host substrate. To overcome this issue, semiconductor industries have periodically used a wafer thinning process called back grinding⁴³ to remove the bulk of the substrate from the back side of the substrate. The abrasive nature of this process can be destructive to fabricated devices thus limiting the final thickness of the substrate down to 50 μ m – resulting in lower flexibility and inhibiting its compliance to an asymmetric soft surface such as the brain. Therefore, one key challenge in developing an integrated system integrating sensors and data management electronics is how to make every piece of electronics flexible.

Other key challenges in building an integrated system for intracranial space are powering and data communication. If the overall system is implanted then the complexity will be much higher requiring powering of the system either by a wireless rechargeable battery or inductive coupling. Data communication will need an antenna design that will need surface area, which will be exceedingly challenging for their placement in the compact intracranial space. Additionally,

the biocompatibility of the materials in the systems is critical. Another important aspect is data volume related to human body especially for brain study is huge and complex (massive simultaneous data generation/sensing) necessitates data management electronics occupying large area (2.5 cm^2). Also, integration of power and data communication devices makes the overall system large enough (cm^2) to be physically compliant.

EXPERIMENTAL

Our project involves heterogeneous integration of soft-materials and silicon based complementary metal oxide semiconductor (CMOS) electronics, RF antenna and a resonance power coupler. For an optimal design we will have the system physically isolated into implantable and epidermal platforms. The implanted portion will have electrodes, counters, analog-to-digital converter, mixer, voltage controlled oscillator, resonant coil to minimize the presence of foreign elements in the intracranial space. The epidermal (on scalp) portion will have the other part of inductive coil to complete the inductive coupling (for power management). The system will be completely wireless. A major thrust for the project is to facilitate flexible systems with data management capability. Successful execution of the project will enable system level integration strategy of ultra-low power interactive advanced healthcare system involving both active and passive elements. Figure 1 shows a conceptual image.

Figure 1: Schematic of the proposed BMI system in its implanted location.

Lowering the power consumption from a device and circuit perspective is a universal goal for any mobile electronics and especially for implantable electronics. We aim to develop our system with total power consumption restricted to 20 mW/cm^2 which will raise the temperature by 1°C which is acceptable for intracranial space.

Spatial geometry of electrodes plays critical role in information gathering. As an example, if neural electrodes need to have an optimal distance of 1.25 mm or smaller for efficient operation in the temporal gyrus and motor cortex⁴⁵. Decoding of motor control signals⁴⁶ and spoken words⁴⁷ needs a spacing of 1 mm or less. If the spacing is $500 \mu\text{m}$ in the occipital cortex, then micro-field evoked potentials can be distinguished from ocular dominance columns⁴⁸. Observation of micro-seizures, micro-discharges and high-frequency oscillations in epileptic brains^{49, 50} needs sub-mm spacing. However, clinically used subdural electrodes are much larger ($\sim 3 \text{ mm}$ in diameter) and maintain large interspacing ($\sim 10 \text{ mm}$) to cover the large surface area of brain ($80 \text{ mm} \times 80 \text{ mm}$) to accurately localize seizure-generating brain regions. Therefore, dramatic scaling using CMOS process for large-scale-integration of neural electrodes is critical to gather many signals very precisely as the brain functions can vary by $\sim 5 \text{ mm}$ across subjects⁵¹⁻⁶¹. Such arrangements were not possible in the past due to the spacing limitation in the intracranial space because of the presence of thousands of wires. Recent studies show initial progress in this direction³⁸. Still an ultra-dense flexible neural electrode array integrated with pertinent data management circuitry, communication medium and power supply in an integrated system is yet to be developed.

RESULTS AND DISCUSSION

In general, many seminal studies have been conducted in the past on ultra-low-power circuit design for BMI system^{62–67}. Previous studies focusing on brain physiology indicates that the maximum tolerable power consumption in the intracranial space is 40 mW/cm^2 , which will allow an increase in temperature of 2°C ⁶⁸. Therefore, we have chosen a total power consumption of 30 mW/cm^2 that is 75% of the maximum allowed power consumption. With a 50% power supply efficiency this will allow us to design a power supply of 60 mW using inductive coupling, which transfers power wirelessly through electromagnetic mutual inductive coupling between two metal coils. Next, we will focus on using 75% of the transmitted power which is equivalent to 22.5 mW/cm^2 . Out of this usable power, we will dedicate 10 mW/cm^2 as usable power (dynamic plus static) by the analog (RF) and digital transistors. Our idea is to use counter blocks (each with 400 transistors) to select a row or a column (Figure 2 – Left). The neural signals will be selected one-at-a-time by raster scan using two shift registers (one for row select and one for column select) driven by 10 MHz clock signal. Thus, the whole 1 cm^2 area will be scanned every 0.1 ms . Then the signals will be individually amplified using a dedicated sense transistor in common-source configuration for each electrode. The output of the transistor will be fed to a 4-bit successive approximation analog-to-digital convertor (ADC) which will consist of 125 logic transistors. For the first system, a 4-bit ADC will be used, since this will provide us with sufficient signal resolution in the digital space. The bit count can be increased to increase output resolution at a later stage (scalability). From there, the digital data will go to a mixer, mounted on the RF signal for wireless transmission. The RF carrier signal will be generated using a voltage controlled oscillator (VCO). Additionally VCO can also serve the purpose of a power amplifier which can cause significant power consumption. Based on the overall circuit design, we find the total power consumption will be within $1\text{--}3 \text{ mW/cm}^2$. That leaves us with at the least $5\text{--}6 \text{ mW/cm}^2$ power which will influence the selection of number electrodes (apart from the fact that there will be a theoretical number of maximum transistors without considering the integration density capability). Each of our transistors consumes $1 \mu\text{W}$ power during dynamic operation and 0.1 nW of static power during the idle state. These data have been collected from nearly 30,000 fabricated transistors at KAUST over the course of 3 years' time in various stages (not from one single experiment). Based on this dataset, we can safely assume a maximum number of 12M transistors/ cm^2 . Since we are dedicating three transistors per electrode for signal acquisition, this is scalable up to 4M electrodes/ cm^2 . This calculation is applicable for $2.5 \text{ mm} \times 2.5 \text{ mm}$ electrodes with $1:1$ pitches for an array of 2000×2000 electrodes. Parasitic loss management will also be possible with such dimensions in the array. Thus, we envision system to have full scaling potential to achieve the “holy grail” envisioned by the US Brain Research through Advancing Innovative Neurotechnologies (BRAIN) initiative.^{69, 70} Yet, we will restrict our development up to 3200 electrodes which will require integration of nearly 12,000 transistors (both digital logic and analog RF). Based on these calculations, we anticipate a total power consumption within 20 mW/cm^2 with further power scaling opportunities from both circuit and device perspective.

Figure 2: Left: Block diagram of the circuitry for data acquisition; Right: Block diagram of the power coupler.

CONCLUSION

We report a pragmatic analytical approach to design implantable electronics. The reported research will open up opportunities for further scientific exploration to impact a broader multi-disciplinary community including (but not limited to): (i) the possibility of making the system transient (dissolvable) eliminating surgical extraction after aimed operation; (ii) a common physically flexible CMOS platform in the general area of implantable electronics for other healthcare applications with minimal changes in the hardware; (iii) new knowledge about the mechanical variability impact on electrical performance and reliability of flexible-stretchable electronics systems for implantable, wearable, epidermal purpose; and (iv) integration opportunity to employ energy harvesting, storage and data storage devices.

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