Matching Properties of Femtofarad and Sub-Femtofarad MOM Capacitors

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Abstract—Small metal-oxide-metal (MOM) capacitors are essential to energy-efficient mixed-signal integrated circuit design. However, only few reports discuss their matching properties based on large sets of measured data. In this paper, we report matching properties of femtofarad and sub-femtofarad MOM vertical-field parallel-plate capacitors and lateral-field fringing capacitors. We study the effect of both the finger-length and finger-spacing on the mismatch of lateral-field capacitors. In addition, we compare the matching properties and the area efficiency of vertical-field and lateral-field capacitors. We use direct mismatch measurement technique, and we illustrate its feasibility using experimental measurements and Monte Carlo simulations. The test-chips are fabricated in a 0.18 μm CMOS process. A large number of test structures is characterized (4800 test structures), which improves the statistical reliability of the extracted mismatch information. Despite conventional wisdom, extensive measurements show that vertical-field and lateral-field MOM capacitors have the same matching properties when the actual capacitor area is considered. Measurements show that the mismatch depends on the capacitor area but not on the spacing; thus, for a given mismatch specification, the lateral-field MOM capacitor can have arbitrarily small capacitance by increasing the spacing between the capacitor fingers, at the expense of increased chip area.

Index Terms—Analog-to-digital converter (ADC), capacitance-to-digital converter (CDC), capacitive digital-to-analog converter (CapDAC), capacitor mismatch, energy-efficient circuits, metal-oxide-metal (MOM) capacitors, mismatch characterization, programmable capacitor array (PCA).

I. INTRODUCTION

CAPACITANCE sets a fundamental limit for the energy consumed in electronic circuitry. The energy required to charge a capacitor (C) to a voltage (V) is given by CV^2 ; thus, the smaller the capacitance the smaller the energy consumed. Energy efficiency of digital circuitry has been steadily

improving by benefiting from the continuous down scaling of the technology minimum feature size. The down scaling results in smaller device capacitances, where the parasitic capacitance of the interconnects is now the limiting factor. On the other hand, for analog and mixed-signal circuitry there are two factors that limit reducing the capacitance, namely, thermal noise and matching [1]. The thermal noise of a simple R-C circuit (e.g., a sampling circuit) is given by kT/C , which imposes a lower bound on the minimum required capacitance to achieve a given signal-to-noise ratio. With respect to matching, a smaller capacitance typically has a smaller area, which results in higher mismatch as given by Pelgrom's inverse-area mismatch model [2].

For low and medium resolution circuits, the minimum capacitance is limited by the mismatch, rather than the thermal noise [3]–[5]. An important application where capacitor matching plays an important role in defining the circuit performance is data-converter circuits [3], [6]–[9]. For instance, in charge-redistribution analog-to-digital converters (ADCs), the matching of the unit capacitors in the capacitive digital-to-analog converter (CapDAC) is the primary factor affecting the ADC linearity [3], [10], [11]. The matching of the unit capacitors also defines the absolute resolution and the dynamic range of successive-approximation capacitance-to-digital converters (CDCs) [8].

Several types of capacitors are used in the design of mixed-signal circuits, e.g., poly-insulator-poly (PIP) capacitors, metal-insulator-metal (MIM) capacitors, and metal-oxide-metal (MOM) capacitors. PIP capacitors have superior area efficiency and matching properties [1], [12]; however, they are no longer supported by semiconductor foundries in technologies beyond 180 nm. MIM capacitors have good area efficiency; however, they are usually associated with strict layout design rules which limit the minimum MIM capacitance to several femtofarads or tens of femtofarads. In addition, MIM capacitors require special dedicated metal layers and process steps; thus, they are not supported by all process technologies. On the other hand, MOM capacitors are built using the standard metal interconnect layers; thus, they can be implemented in any digital CMOS process. In addition, MOM capacitors can be custom-crafted as layout parasitic elements; thus, they can be arbitrarily small, where the layout design rules to be observed are merely the metal-width and metal-spacing rules of the interconnect layer [3], [9].

In spite of the importance of small MOM capacitors in the design of energy-efficient mixed-signal circuits, only few reports discuss their matching properties based on reliable measurement data. The effect of the finger-length of lateral-field MOM capacitor on mismatch is reported in [13] using two test structures (1.2 fF and 0.45 fF). The mismatch measurement technique used in [13] employs a dedicated on-chip ADC for every

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instance of the test structures, which requires considerable design-time and silicon area and makes it difficult to port the test structure from one technology to another. Matching properties of MOM capacitors down to 8 fF are reported in [14]. However, the mismatch measurement technique used in [14] relies on a complicated and error-prone process where component values are tuned in simulation till simulation results fit with measurement data.

In this paper, we study the matching properties of parallel-plate (vertical-field) and fringing (lateral-field) MOM capacitors using eight different test structures with unit capacitance down to 0.5 fF. The effect of both the finger-length and finger-spacing of fringing MOM capacitors on mismatch is studied. Direct mismatch measurement technique is employed, which allows simple and accurate mismatch measurement [1]. Six test-chips fabricated in a 0.18 μm CMOS process and comprising a total of 4800 test structures are characterized. Measured results show that the mismatch of both vertical-field and lateral-field MOM capacitors follow Pelgrom's inverse-area model. The matching properties of vertical-field and lateral-field MOM capacitors are compared, and it is demonstrated that—despite conventional wisdom—both have the same matching properties when the actual capacitor area is considered. Measurements show that a given matching requirement can be achieved using arbitrarily small capacitance by increasing the spacing while keeping the capacitor area constant. The area efficiency of vertical-field and lateral-field capacitors is compared, and the conditions that can make one type of implementation preferable are discussed.

The remainder of this paper is organized as follows. Section II explains the direct mismatch measurement technique and demonstrates its feasibility using experimental measurements and Monte Carlo simulations. Section III describes the capacitive test structures used in this study and illustrates the reliability of the proposed mismatch measurement approach using Monte Carlo simulations. Section IV presents experimental results and provides insights on the measured matching properties of vertical-field and lateral-field MOM capacitors. Section V concludes this paper.

II. DIRECT MISMATCH MEASUREMENT

A simplified schematic illustrating direct mismatch measurement is shown in Fig. 1. A pair of matched capacitors (C_{eq1} and C_{eq2}) is directly measured using an LCR meter. By using on-chip switches, only one capacitor is connected to the LCR meter at a time. The difference between the two LCR meter readings is the mismatch between the two capacitors. This process is applied to several identical pairs of matched capacitors to generate a statistical distribution that can be used to calculate the standard deviation of the mismatch between C_{eq1} and C_{eq2} . In order to increase the absolute capacitance difference to be measured by the LCR meter, each of C_{eq1} and C_{eq2} is comprised of N_E independent unit capacitors (C) connected in parallel. Thus, the absolute standard deviation to be measured is given by

$$\sigma(C_{eq}) = \sqrt{N_E} \times \sigma(\Delta C) \quad (1)$$

Fig. 1. Simplified schematic illustrating direct mismatch measurement between one pair of capacitors (C_{eq1} and C_{eq2}). The parasitic capacitance at the HIGH and LOW terminals are denoted as $C_{P,H}$ and $C_{P,L}$, respectively.

Fig. 2. Results of Monte Carlo simulation showing the percent of error in the capacitance mismatch measurement due to the mismatch in the switch ON resistance vs. the number of unit capacitors connected in parallel (N_E). The parameters used for simulation are as follows: $C = 1$ fF, $\sigma(\Delta C/C) = 0.2\%$, and 1 MHz measurement frequency.

where ΔC is the random variation of the unit capacitor (C). The standard deviation of the unit capacitor relative variation is denoted as $\sigma(\Delta C/C)$.

The first possible source of error in the previously described measurement configuration is the mismatch in the ON resistance of the switches used to select the capacitor-under-test. However, noting that the capacitor-under-test is in the femtofarad range, the ON resistance is negligible compared to the capacitor reactance, where frequencies used in precision LCR meters are typically ≤ 1 MHz. To further illustrate this, Monte Carlo circuit simulation was performed using the models provided in the 0.18 μm process used to implement the test-chips in this study. The worst case error occurs when the reactance of the capacitor-under-test is small (i.e., large number of elements and large measurement frequency) and the switch ON resistance is large (i.e., small transistor width). Fig. 2 shows that even when using a small switch of $W/L = 0.5 \mu\text{m}/0.18 \mu\text{m}$, a large number of elements ($N_E = 50$), and a large measurement frequency of 1 MHz, the error is less than 0.01%. Thus, the error due to the switches ON resistance mismatch is practically negligible.

Fig. 3. Standard deviation of measurement noise vs. number of averaged LCR meter readings (N_{avg}) plotted on a log-log scale. The data set is obtained from 30 000 consecutive LCR meter readings of a 2 fF unit capacitor with $N_E = 6$.

The second possible source of error is the parasitic capacitance at the two terminals of the capacitor-under-test. Parasitic capacitances at the HIGH and LOW terminals of the LCR meter are denoted as $C_{P,H}$ and $C_{P,L}$, respectively, as shown in Fig. 1. $C_{P,H}$ does not affect the measurement because the measured current is the current flowing into the current-to-voltage converter (I-to-V) at the LOW terminal. The LCR meter LOW terminal is a virtual ground; thus, $C_{P,L}$ does not affect the measurement in the ideal case. Moreover, the LOW terminal is connected to the common terminal of C_{eq1} and C_{eq2} ; thus, the same parasitic capacitance exists when performing the two measurements. Consequently, even if $C_{P,L}$ affects the measurement due to non-ideal effects, it will affect the measurement of C_{eq1} and C_{eq2} equally; thus, it will not affect the mismatch measurement. In addition, the parasitic capacitance is actually dominated by the capacitance of the cables, connectors, and pads; thus, any mismatch in the parasitic capacitance of the on-chip switches or the capacitor-under-test is practically negligible.

Given the previous two arguments, the only limitation to the direct mismatch measurement technique is the measurement accuracy of the LCR meter itself. For capacitors in the femtofarad range, the absolute accuracy of commercial LCR meters is worse than 1%. Therefore, if we assume a 2 fF unit capacitor with $\sigma(\Delta C/C) = 0.1\%$, it may be anticipated that such a measurement cannot be directly performed with an LCR meter. However, the purpose of mismatch measurement is to quantify the difference between two consecutively measured capacitors, rather than measuring the absolute value of the capacitance. Thus, the important specification that affects mismatch measurement is the short-term repeatability (i.e., measurement noise) rather than the absolute accuracy.

In order to illustrate the feasibility of direct mismatch measurement, Fig. 3 shows the rms noise when measuring one of the capacitive structures fabricated in this study, using a commercial LCR meter (Agilent E4980A). The rms noise is only 11 aF which is much better than the absolute accuracy, and it can be reduced by averaging multiple readings. Fig. 3 shows that the rms noise is inversely proportional to $\sqrt{N_{\text{avg}}}$, where N_{avg} is the number of averaged readings [15]. By averaging 100 readings an rms noise as low as 1 aF can be obtained.

III. CAPACITIVE TEST STRUCTURES

Two types of MOM capacitors are considered in this work. The first type is a vertical-field parallel-plate capacitor using

Fig. 4. Simplified schematic of (a) the vertical-field parallel-plate capacitor, and (b) the lateral-field fringing capacitor used in the mismatch study.

Metal5 and Metal4 layers as shown in Fig. 4(a). The capacitor area is L^2 , where L is the side length of the overlap region. The vertical spacing between Metal5 and Metal4—i.e., the interlayer dielectric thickness (T_{OX})—is $\approx 0.55 \mu\text{m}$. The connections to the bottom plates were made using Metal2 layer, while Metal3 layer was used as a shield to eliminate any parasitic capacitance between the routing wires and the top plate. The second type is a lateral-field fringing capacitor built using interdigitated fingers in Metal5 layer as shown in Fig. 4(b). The capacitor is defined by three parameters: the overlap length (L), the width of the metal finger (W), and the spacing between the fingers (S). The thickness of the metal layer (T_M) is $\approx 0.48 \mu\text{m}$.

Fig. 5 shows a simplified schematic of the implemented test-chip. Three sets of capacitors (A, B, and C) were considered in the study. Each set comprises three arrays of test structures: e.g., set A comprises the arrays A1, A2, and A3. Each array is comprised of 100 identical test structures: e.g., as shown in Fig. 5, the array A1 has 100 structures from A1[1] to A1[100]. Each test structure, e.g., A1[1], has two matched capacitors: C_{eq1} and C_{eq2} . Using on-chip switches, only one capacitor is connected to the CTOP and CBOT terminals at a time. The LCR meter measures the mismatch between the two capacitors (C_{eq1} and C_{eq2}) in each test structure. The on-chip switches are controlled by a register file which is accessed through an SPI interface.

Each capacitor (C_{eq1} or C_{eq2}) is comprised of N_E unit capacitors connected in parallel: i.e., N_E elements. The pitch between elements is $\geq 2.72 \mu\text{m}$; thus, the assumption of independent unit capacitors in (1) is fairly reasonable [3], [13]. The rationale behind choosing the number of elements per capacitor is to keep $\sigma(C_{\text{eq}})$ given by (1) sufficiently above the LCR meter noise level. In addition, the number of elements was tuned to ensure a symmetric layout to minimize systematic mismatch.

The parameters of the test structures are summarized in Table I. Unit capacitors of three different values were considered: namely, 2 fF, 1 fF, and 0.5 fF. Set A has three arrays of structures (A1, A2, and A3) of the vertical capacitor shown in Fig. 4(a).

Fig. 5. Simplified schematic of the implemented test-chip. Each array is comprised of 100 identical mismatch structures. Each mismatch structure contains two matched capacitors (C_{eq1} and C_{eq2}).

TABLE I
PARAMETERS OF THE TEST STRUCTURES USED IN THE MISMATCH STUDY. SET A COMPRISES VERTICAL-FIELD CAPACITORS WITH DIFFERENT SIDE LENGTHS (L), SET B COMPRISES LATERAL-FIELD CAPACITORS WITH LENGTH (L) VARIED WHILE SPACING (S) IS CONSTANT, AND SET C COMPRISES LATERAL-FIELD CAPACITORS WITH SPACING (S) VARIED WHILE LENGTH (L) IS CONSTANT

	Type	Unit Cap (C) (fF)	No. of elements (N_E)	Equivalent Cap (C_{eq}) (fF)	L (μm)	W (μm)	S (μm)	Unit Cap Chip Area (μm^2)
A1	Vertical	2	6	12	5.12	-	-	26.2
A2		1	21	21	3.42	-	-	11.7
A3		0.5	80	40	2.32	-	-	5.4
B1	Lateral	2	6	12	11.84	0.36	0.32	16.1
B2		1	20	20	5.92	0.36	0.32	8.0
B3		0.5	80	40	2.96	0.36	0.32	4.0
C1	Lateral	2	6	12	11.84	0.36	0.32	16.1
C2		1	20	20	11.84	0.36	0.76	26.5
C3		0.5	80	40	11.84	0.36	1.55	45.2

The side length (L) of the unit capacitor is varied in the layout and a parasitic extraction tool (Mentor Calibre) is used to verify that the three aforementioned values of unit capacitors are achieved. Similarly, Set B has three arrays of structures (B1, B2, and B3) of the lateral capacitor shown in Fig. 4(b), where the finger spacing (S) is constant while the overlap length (L) is varied. Set C also has three arrays of lateral structures (C1, C2, and C3) but the overlap length (L) is constant while the spacing (S) is varied. Structures B1 and C1 have the same parameters; thus, they are physically implemented as one array, i.e., a total of eight arrays are implemented in the test-chip.

In order to investigate the effect of the LCR meter noise on the mismatch measurement, a MATLAB Monte Carlo simulation was conducted. Without loss of generality, the simulation used the parameters of structures B1 and B2 where it was assumed that $\sigma(\Delta C/C)$ of B1 and B2 is 0.15% and 0.2%, respectively. For both B1 and B2, $\sigma(\Delta C/C)$ was estimated from 100 mismatch structures, which is the same number of structures per array per test-chip. Based on the measurement data in Section II, the LCR meter rms noise is assumed to be ≈ 11 aF. Fig. 6 shows that as the number of averaged readings increases, the effect of the noise becomes negligible and the estimated $\sigma(\Delta C/C)$ converges to the expected values. It may be anticipated that a large number of readings, and consequently long measurement time, is required; however, even when using a small number of readings, the effect of the LCR meter noise

Fig. 6. Monte Carlo simulation results to illustrate the effect of LCR meter noise on the estimated $\sigma(\Delta C/C)$. The estimated $\sigma(\Delta C/C)$ is plotted vs. the number of averaged LCR meter readings (N_{avg}).

can be subtracted from the estimated $\sigma(\Delta C/C)$ to obtain a corrected estimate that is given by

$$\sigma_{\text{corrected}}\left(\frac{\Delta C}{C}\right) = \sqrt{\sigma_{\text{noisy}}^2\left(\frac{\Delta C}{C}\right) - \frac{\sigma_{\text{noise}}^2}{N_{\text{avg}}}} \quad (2)$$

where σ_{noise}^2 is the LCR meter rms noise. As shown in Fig. 6, by averaging 10 readings only the corrected $\sigma(\Delta C/C)$ is close to the expected value; however, 100 readings were averaged in the experimental measurements to further improve the accuracy of the results.

Fig. 7. Monte Carlo simulation results for the estimated $\sigma(\Delta C/C)$ using six chips where each chip contains 100 mismatch structures.

Fig. 8. Micrograph of the fabricated MOM mismatch characterization test-chip.

The statistical distribution of the test structures mismatch measurement is used to estimate $\sigma(\Delta C/C)$. The larger the number of measured test structures, the smaller the error in the estimated $\sigma(\Delta C/C)$. To obtain an estimate of the expected error in the estimated $\sigma(\Delta C/C)$, an additional Monte Carlo simulation was performed. Without loss of generality, the simulation emulates the measurement scenario of the structure B2, assuming its $\sigma(\Delta C/C)$ to be 0.2%. Each chip has 100 mismatch structures of B2, where each structure is measured 100 times. After averaging the readings of each structure and subtracting the LCR meter noise, $\sigma(\Delta C/C)$ is estimated from the resulting distribution. Furthermore, the simulation assumes that a total of six chips are characterized (which is same number of experimentally characterized chips); thus, the estimated standard deviations from the six chips are averaged to obtain a more accurate estimate of $\sigma(\Delta C/C)$. The Monte Carlo simulation repeats the previous scenario 1000 times, and the resulting distribution of the estimated $\sigma(\Delta C/C)$ is shown in Fig. 7. The mean of the distribution is very close to the actual value (0.2%) and the rms error is only 0.006%, which illustrates the accuracy of the measurement scenario employed in this study.

IV. RESULTS AND DISCUSSION

A. Fabricated Chip and Test Setup

Fig. 8 shows a micrograph for the test-chip fabricated in a 0.18 μm CMOS technology. All the mismatch structures are covered with a metal shield using the top metal layer (Metal6). The fabricated chips were directly mounted on custom test

Fig. 9. Schematic of the test setup used for mismatch characterization.

Fig. 10. Measured $\sigma(\Delta C/C)$ for structures B1 and B2 vs. number of averaged readings.

Fig. 11. Repeatability of the measured $\sigma(\Delta C/C)$ for three test structures: A1, B1/C1, and B2.

boards and 65 $\mu\text{m} \times 65 \mu\text{m}$ pads were directly bonded to the board using Hybond 676 wedge wire bonder. A large number of digital signals is used on-chip to control the switches associated with the large number of structures; however, by implementing an SPI interface, the number of the chip digital input/output signals were minimized. A total of six chips were characterized in this study: i.e., 600 mismatch measurement points for each type of structure and 4800 total mismatch measurement points. Noting that each structure has two capacitors and each measurement point is obtained by averaging 100 readings, a total of 960 000 readings were performed. A LabVIEW program was designed for measurement automation and data acquisition. An Aardvark USB-to-SPI adapter is used to communicate with the test-chip. Data acquisition from the LCR meter is done via GPIB. The LCR meter is connected to the test board using shielded cables and SMA connectors. Fig. 9 shows a schematic of the test setup.

Fig. 12. Histograms of the measured relative variation ($\Delta C/C$) for each type of mismatch structures using one test-chip. Set A has vertical capacitors with length (L) as a variable, set B has lateral capacitors with length (L) as a variable, and set C has lateral capacitors with spacing (S) as a variable. Capacitor values for each set are 2 fF, 1 fF, and 0.5 fF.

B. Averaging and Repeatability

The effect of the LCR meter noise on the estimated $\sigma(\Delta C/C)$ was experimentally verified. As an example, the estimated $\sigma(\Delta C/C)$ from measurement data of structures B1 and B2 is plotted vs. number of averaged readings in Fig. 10. The measured results show the same behavior expected from the Monte Carlo simulations shown in Fig. 6. By correcting $\sigma(\Delta C/C)$ using (2), a fairly accurate estimate can be obtained using a small number of readings. However, for all the reported results, 100 readings were averaged for each mismatch measurement point to improve the accuracy and the reliability of the measurements.

To further demonstrate the robustness of the measurement technique used in this study, the repeatability of the measurement was assessed by repeating the measurement on the same array for 10 times. As an example, Fig. 11 shows the estimated $\sigma(\Delta C/C)$ for three different arrays (A1, B1/C1, and B2) on one test-chip for 10 measurement cycles, where the results show excellent repeatability.

C. Measured Capacitor Variation

Fig. 12 shows the histograms of the measured relative variation of each type of test structure from one test-chip. For structures of set A and set B, the estimated $\sigma(\Delta C/C)$ matches the expected behavior from Pelgrom's inverse-area model: the smaller capacitors (with smaller area) show higher relative variation. For set C, although the three structures have different unit capacitors (2 fF, 1 fF, and 0.5 fF) and occupy different chip areas, they all show similar relative variation. The measurement

procedure is repeated for six chips, and the estimated $\sigma(\Delta C/C)$ is plotted vs. chip index in Fig. 13. The measurements of each set are grouped together in a subfigure. The behavior observed in Fig. 12 is similar for all the chips: i.e., the structures of set A and set B follow Pelgrom's inverse-area relation, while structures of set C have almost the same $\sigma(\Delta C/C)$. The explanation for this behavior follows in the next subsection.

D. Pelgrom's Coefficients

The previous results can be explained by noting that Pelgrom's inverse-area dependence is based on the area of the capacitor itself rather than the occupied top-view chip area or the value of the capacitance. The analysis of capacitance errors due to random oxide variations shows that $\sigma(\Delta C/C)$ satisfies [16, eq. (16)]

$$\sigma\left(\frac{\Delta C}{C}\right) \propto \frac{1}{\sqrt{A}} \cdot \sqrt{\sigma^2\left(\frac{\Delta \epsilon_r}{\epsilon_r}\right) + \sigma^2\left(\frac{\Delta S}{S}\right)} \quad (3)$$

where A is the capacitor area and ϵ_r is the oxide relative permittivity. For set C of lateral capacitors, the capacitor area is the lateral area, which is the same for the three structures: C1, C2, and C3. The measurement results in Figs. 12 and 13 show that the structures of set C have the same mismatch behavior, which means that $\sigma(\Delta C/C)$ does not depend on S . Hence, the dominant component in (3) is $\sigma^2(\Delta \epsilon_r/\epsilon_r)$ rather than $\sigma^2(\Delta S/S)$, and (3) simplifies to the well-known Pelgrom's inverse-area relation. This also suggests that vertical capacitors and lateral capacitors should show the same mismatch behavior

Fig. 13. Measured $\sigma(\Delta C/C)$ for the structures of six different chips. From left to right: set A of vertical capacitors with length (L) as a variable, set B of lateral capacitors with length (L) as a variable, and set C of lateral capacitors with spacing (S) as a variable. Capacitor values for each set are 2 fF, 1 fF, and 0.5 fF.

TABLE II
MEASURED UNIT CAPACITOR MEAN VALUES, MEAN $\sigma(\Delta C/C)$, AND PELGROM'S COEFFICIENTS EXTRACTED BY CURVE FITTING

	Type	Unit Cap (C) (fF)	$\sigma\left(\frac{\Delta C}{C}\right)$	$K_{A,top}$	$K_{A,lateral}$	K_C
A1	Vertical	1.95	0.10%	$0.49\% \cdot \mu m$	-	$0.14\% \cdot \sqrt{fF}$
A2		0.94	0.15%	RMSE = 0.006%		
A3		0.48	0.21%			
B1	Lateral	1.99	0.14%	$0.57\% \cdot \mu m$	$0.48\% \cdot \mu m$	$0.20\% \cdot \sqrt{fF}$
B2		1.02	0.19%	RMSE = 0.004%		
B3		0.53	0.28%			
C1	Lateral	1.99	0.14%	$0.57\% \cdot \mu m$	$0.48\% \cdot \mu m$	$0.20\% \cdot \sqrt{fF}$
C2		1.03	0.13%	$0.70\% \cdot \mu m$		$0.14\% \cdot \sqrt{fF}$
C3		0.45	0.14%	$0.92\% \cdot \mu m$		$0.10\% \cdot \sqrt{fF}$

when the actual capacitor area is considered, as will be shown in the next subsection.

For set A of vertical capacitors, the capacitor area is itself the top-view chip area; thus, Pelgrom's relation can be written as

$$\sigma\left(\frac{\Delta C}{C}\right) = \frac{K_{A,top}}{\sqrt{A_{top}}} \quad (4)$$

where $K_{A,top}$ is Pelgrom's coefficient for the dependence of $\sigma(\Delta C/C)$ on the top-view chip area (A_{top}). For set B and set C of lateral capacitors, the capacitor area is the lateral area rather than the top-view chip area; thus, Pelgrom's dependence can be written as

$$\sigma\left(\frac{\Delta C}{C}\right) = \frac{K_{A,lateral}}{\sqrt{A_{lateral}}} \quad (5)$$

where $K_{A,lateral}$ is Pelgrom's coefficient for the dependence of $\sigma(\Delta C/C)$ on the lateral area ($A_{lateral}$). Noting that for set B the metal spacing (S) and the metal thickness (T_M) are constant while the length (L) is varied, the top-view area is proportional to the capacitor area; thus, (4) can be applied to set B as well. For both set A and set B, the capacitance is proportional to the capacitor area; thus, a third form of Pelgrom's model can be used, which is given by [13]

$$\sigma\left(\frac{\Delta C}{C}\right) = \frac{K_C}{\sqrt{C}} \quad (6)$$

where K_C is Pelgrom's coefficient for the dependence of $\sigma(\Delta C/C)$ on the capacitance. If (4) and (6) are applied to set C, each structure will have its own Pelgrom's coefficient because the top-view chip area and the capacitance are not proportional to the actual capacitor area.

Pelgrom's coefficients given in (4)–(6) were extracted using non-linear least squares curve fitting, performed using MATLAB curve fitting toolbox. Table II shows the measured mean unit capacitance, mean $\sigma(\Delta C/C)$, and the fitted Pelgrom's coefficients for each structure. Three points were used for the fitting of set A and set B model, where the rms error (RMSE) of the fit is only 0.004% for set A and 0.006% for set B. It is worth mentioning that the increased mismatch due to edge effects reported for the PIP structures in [1] was not observed for the MOM structures in this study.

E. Comparison and Discussion

In order to gain more insight into the results, the measured mean $\sigma(\Delta C/C)$ is plotted vs. capacitance and overlaid on fitted Pelgrom's model in Fig. 14. Fig. 14(a) shows that for the same capacitance value, set A has lower mismatch compared to set B. It may be anticipated from this result that vertical capacitors match better than lateral capacitors; however, this is not true as will be shown shortly. Fig. 14(b) shows that all capacitors of set C have roughly the same $\sigma(\Delta C/C)$ although their capacitor values are different. Taking a horizontal line in Fig. 14(b) reveals that for a given mismatch requirement the capacitance of a lateral capacitor can be arbitrarily small, while taking a vertical line shows that for a given capacitance the mismatch can be arbitrarily small. The price paid in both cases is increasing the occupied chip area.

The relation between vertical and lateral capacitors can be understood with the help of Fig. 15, where the measured mean $\sigma(\Delta C/C)$ is plotted vs. area overlaid on fitted Pelgrom's model. Fig. 15(a) shows that, when the top-view chip area is considered, set A matches better similar to Fig. 14(a). However, when the actual capacitor area is considered (where the capacitor

Fig. 14. Measured mean $\sigma(\Delta C/C)$ vs. capacitance for the three sets of structures overlaid on fitted Pelgrom's model. (a) Set A compared to set B and (b) set B compared to set C.

Fig. 15. Measured mean $\sigma(\Delta C/C)$ vs. area for the three sets of structures overlaid on fitted Pelgrom's model. (a) Set A compared to set B, and (b) all results overlaid vs. actual capacitor area. The x-axis is either top-view chip area or lateral area as indicated in the legend of the subfigures.

area of set B is the lateral area), interestingly, set A and set B almost coincide. This means that, when the actual capacitor area is considered, both vertical and lateral capacitors have the same mismatch behavior when they are implemented using the same process. This is further clarified in Fig. 15(b), which shows that, when the actual capacitor area is considered—which is the lateral area for set B and set C—all the structures of

set A, B, and C follow the same mismatch curve. Previous reports suggested that lateral capacitors should match better than vertical capacitors, because their spacing is determined by accurate lithography [13], [17]. However, based on the presented measurement results, the claim that lateral capacitors match better is disproved. This can be further explained by noting that the dominant component in (3) is $\sigma^2(\Delta\epsilon_r/\epsilon_r)$ rather than $\sigma^2(\Delta S/S)$; thus, the accuracy of the lithography should imply no difference between vertical and lateral capacitors.

Additional experimental measurements for test-chips fabricated in several different technology nodes are required to verify that the above conclusions will remain valid under technology scaling. However, it should be noted that the pitch of top metal layers is typically much larger than the technology minimum feature size [13], [18]. Since top metal layers have less parasitics, they are typically preferred for capacitor implementation. Thus, we expect that the conclusions drawn in this study will remain valid.

F. Area Efficiency

Although the results show that vertical and lateral capacitors will show the same mismatch behavior if the actual capacitor area is considered, an important question is not yet answered: namely, which type of capacitor to use and when? The answer to this question depends on the specific parameters of each process; however, we will present a simplified analysis that uses the parameters of the process used to implement the test-chip as an example. The primary factor affecting the answer is the area efficiency: i.e., given the same capacitance value and the same $\sigma(\Delta C/C)$, which type of capacitor occupies a smaller silicon area?

To answer this question, we assume a vertical capacitor and a lateral capacitor with the same capacitance and the same $\sigma(\Delta C/C)$. From the condition that the two capacitors have the same $\sigma(\Delta C/C)$, it follows that they have the same capacitor area, which can be written as

$$L_V^2 = 2N_M T_M L_L \quad (7)$$

where L_V is the side length of the vertical capacitor, N_M is the number of metal layers used to implement the lateral capacitor, and L_L is the length of the lateral capacitor. Noting that the capacitor area is the same, the condition that the two capacitors have the same value means that they have the same spacing between the capacitor plates. This can be written as

$$N_{OX} T_{OX} = S \quad (8)$$

where N_{OX} is the number of oxide layers between the plates of the vertical capacitor. From (7) and (8), the ratio between the occupied chip area of the vertical capacitor and the lateral capacitor is given by

$$\mu_{\text{Area}} = \frac{L_V^2}{2L_L(W + S)} = \frac{N_M T_M}{W + N_{OX} T_{OX}} \quad (9)$$

where for $\mu_{\text{Area}} < 1$, the vertical capacitor is more area efficient, while for $\mu_{\text{Area}} > 1$ the lateral capacitor is more area efficient. The number of oxide layers (N_{OX}) is practically limited to one or two layers, because at least two metal layers

Fig. 16. Ratio between the occupied silicon area of vertical capacitor and lateral capacitor having the same capacitance value and the same $\sigma(\Delta C/C)$ vs. the number of metal layers used in the lateral capacitor (N_M).

are required for shielding and routing below the capacitor bottom plate layer. On the other hand, the number of metal layers in a lateral capacitor can be as large as the number of the standard routing metal layers in the process. Plotting (9) reveals that, if both N_{OX} and N_M are equal to one, the area efficiency of the vertical capacitor is two times better than the lateral capacitor, as shown in Fig. 16. However, the lateral capacitor is more area efficient in the case of a large number of metal layers: i.e., roughly speaking, when $N_M > N_{OX} + 1$. Technology scaling decreases W and increases T_M [18]; thus, it will be in favor of lateral capacitors. It should be noted that the previous analysis is simplified, e.g., it ignores the effect of vias on lateral capacitors, and it assumes ϵ_r is the same for both vertical and lateral capacitors. Practically, the layout design rules, routing complexity, and parasitics may also affect the designer's choice between vertical and lateral capacitors.

V. CONCLUSION

The mismatch of several different vertical-field and lateral-field MOM capacitors was directly measured using simple test structures that can be automated and ported. A large number of structures is multiplexed using shared pads, which greatly simplifies the testing process and enables extracting mismatch information from reliable statistical distributions. Extensive experimental measurements reveal several important results that are useful to the designer: 1) femtofarad and sub-femtofarad vertical and lateral capacitors follow Pelgrom's inverse-area model, 2) capacitor mismatch depends on the capacitor area but not on the spacing, 3) vertical and lateral capacitors have the same matching properties if the actual capacitor area is considered, 4) vertical capacitors are more area efficient than lateral capacitors that are built using a single metal layer, 5) lateral capacitors are more area efficient if a large number of metal layers are stacked, and 6) for a given matching requirement, the capacitance of a lateral capacitor can be made arbitrarily small by increasing the spacing between the capacitor fingers at the expense of increased chip area.

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