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High performance high- κ /metal gate complementary metal oxide semiconductor circuit element on flexible silicon

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Thinned silicon based complementary metal oxide semiconductor (CMOS) electronics can be physically flexible. To overcome challenges of limited thinning and damaging of devices originated from back grinding process, we show sequential reactive ion etching of silicon with the assistance from soft polymeric materials to efficiently achieve thinned (40 μm) and flexible (1.5 cm bending radius) silicon based functional CMOS inverters with high- κ /metal gate transistors. Notable advances through this study shows large area of silicon thinning with pre-fabricated high performance elements with ultra-large-scale-integration density (using 90 nm node technology) and then dicing of such large and thinned (seemingly fragile) pieces into smaller pieces using excimer laser. The impact of various mechanical bending and bending cycles show undeterred high performance of flexible silicon CMOS inverters. Future work will include transfer of diced silicon chips to destination site, interconnects, and packaging to obtain fully flexible electronic systems in CMOS compatible way. © 2016 AIP Publishing LLC. [<http://dx.doi.org/10.1063/1.4943020>]

Bulk mono-crystalline silicon (100) based complementary metal oxide semiconductor (CMOS) electronics have served as critical catalysts for today's digital world. Moving forward, as we embrace Internet of Everything where integration of people, process, device, and data will enhance connectivity and quality of life, a physically flexible form of silicon CMOS can be game changer. It is like adding fifth dimension to their existing quadruple advantages: high performance, relative energy efficiency, ultra-large-scale-integration (ULSI) density, and performance per cost. However, one major challenge to realize flexible CMOS electronics is silicon is rigid and brittle. Fundamentally, thinning the silicon can reduce its flexural rigidity making it flexible.¹ Therefore, various processes have been developed to thin down the silicon substrate.^{2–26} Such processes include either a top-down approach to lift-off the full or the small localized area of the silicon or a bottom-up approach to reduce the silicon substrate's thickness from the bottom. For the former approach, frequently, expensive substrates like silicon-on-insulator (SOI) have been used. Also, expensive and complex processes like porosity formation, high energy ion implantation, epitaxial growth, and metal assisted stressor based spalling have been used.^{27–30} The main advantage is potentially the remaining substrate can be reused.

Compared to that, one fundamental challenge of bottom-up approach is cost, as the bulk portion of the substrate is lost or wasted during the process. However, the key advantage of this approach is retention of the whole effective substrate area for ULSI. Therefore, in the semiconductor industry, abrasive substrate back-grinding is commonly used. Due to its severe mechanical nature, this process often

damages the pre-fabricated devices and is self-limited in terms of minimum thickness that can be achieved. To overcome this challenge of partial flexibility, recently, we have demonstrated sequential reactive ion etching (RIE) based silicon substrate thinning.² As step forward toward fully flexible electronic systems here we show: (i) dicing of such thinned silicon substrate with pre-fabricated devices and (ii) functionality of flexible CMOS circuitry made with advanced high- κ /metal gate stacks under various mechanical operations. Since CMOS circuitry is built by physical interconnections of many wires and devices, in-depth study of the impact of various mechanical bending conditions on the flexible CMOS circuitry is imperative to understand the scalability and boundary of this process.

We started with an 8 in. bulk mono-crystalline p-type silicon (100) substrate (10^{15} atoms/cm³) using state-of-the-art gate first flow. First, we formed the wells using standard ion implantation processes. Then, we isolated the active areas by forming shallow trench isolation (STI). Next, we deposited the gate stack with 3 nm hafnium oxide (HfO₂) as gate dielectric, and 10–20 nm titanium nitride as metal gate and 100 nm poly-crystalline silicon. Then, we patterned the gate of the devices. Next, we formed silicon nitride (Si₃N₄) spacers on the gate sidewalls in order to protect the gate from future implantation and salicidation processes. Then, we formed the source and drain using two different lithography and implantation processes. After that, we performed S/D activation anneal on the fabricated circuits at 1000 °C for 10 s. Next, we formed the nickel silicide (NiSi) on the source and drain regions creating ohmic contact on the test pads and the gate, source and drain regions. Finally, we performed forming gas anneal (FGA) using a combination of nitrogen/hydrogen (N₂/H₂) at 420 °C to remove trapped charges. The process to thin down the silicon substrate (800 μm thick)

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starts by protecting the fabricated devices with thick ($7\text{ }\mu\text{m}$) photoresist. Next, the back surface was etched using RIE to reduce the thickness of the substrate and obtain the required flexibility. We divided the back-etching process into four different stages in order to control the substrate thickness between each of them. The first stage reduces the thickness from $800\text{ }\mu\text{m}$ to $300\text{ }\mu\text{m}$. Then, we control the thickness with mechanical and optical profilers. Next, we reduced the substrate thickness in 3 more etch steps until we obtain the target of $30\text{--}40\text{ }\mu\text{m}$. At this point, the platform is thin enough to be flexible and can be easily bent down to 2 cm bending radius; at this bending radius, the applied strain at the top surface of the chip can be calculated by

$$\varepsilon_{nom} = \frac{t}{2R}, \quad (1)$$

where ε_{nom} is the nominal strain applied to the top surface of the sample, t is the final thickness of the flexible chip, and R is the bending radius. Using formula (1), the applied strain on the surface of the sample was found to be 0.001% . When we reached the desired thickness, we removed the photoresist layer from the top using acetone and isopropanol. To dice the etched samples, we used $1.06\text{ }\mu\text{m}$ ytterbium-doped fiber laser (PLS6MW Multi-Wavelength Laser Platform, Universal Laser Systems, USA). The laser-based dicing enabled us to dice the etched samples easily in any shape precisely. We calibrated power, speed, and frequency parameters for the laser just to get enough marking on the sample where we then gently cleaved it by hand. We also found out that backside dicing is better compared to the front side dicing since it does not leave any laser engravings on the top surface. Fig. 1(a) shows the fabricated devices at a 2 cm bending radius. In order to confirm the final substrate thickness, we performed scanning electron microscopy (Fig. 1(b)). Figure 1(c) shows an optical profilometer measurement of the back surface confirming that no scallop pattern has been created as in our previously reported works.¹³ Fig. 1(d) depicts an SEM image of the fabricated CMOS based inverters. Fig. 1(e) shows the silicon substrate after each etch step, confirming the silicon thickness reduction. Figures 1(f)

and 1(g) show digital images of the devices before and after laser dicing.

All the characterized inverters consisted of one NMOS transistor with a gate length of 250 nm and 350 nm channel width and one PMOS transistor with a gate length of 250 nm and a channel width of 450 nm . Even though we have been able to fabricate discrete CMOS devices with 90 nm gate lengths (L), inverters were fabricated with higher gate lengths in order to prevent short channel effects due to threshold shift. We started the characterization by testing the devices before flexing (mechanical bending) process to establish the reference to gauge the performance deviation after bending. We characterized all the inverters using a semi-automatic probe station at three different states: flat, bent in downward direction (tensile stress), and bent in upward direction (compressive stress). Fig. 2 shows the transfer and output curves of the characterized transistors at 2 cm bending radius. The NMOS transistor parameters were calculated at $V_{dd} = 50\text{ mV}$ and show a threshold voltage (V_{th}) of 0.2 V , mobility of $132\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$, and a subthreshold swing (SS) of 80 mV/dec . The PMOS transistor shows a V_{th} of -0.25 V , mobility of $80\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$, and SS of 75 mV/dec . We began the inverter characterization with DC analysis of the circuit to obtain the voltage transfer curve (VTC). For this, we applied a DC voltage sweep to the input port of the inverter while V_{DD} and kept the ground constant at 1 V and 0 V , respectively. The obtained curves for the characterized inverter in flat, bending downward, and bending upward show no change in the performance of the circuit (Figs. 3(a)–3(c)). To completely understand the DC behavior of the inverter, the switching threshold (V_M) was obtained from the VTC plot at the point where $V_{out} = V_{in}$. The obtained values for V_M were 0.40 V for bulk sample, 0.39 V for all bending downwards radii, and 0.41 V for all bending upwards radii. Also, the gain of the inverter can be obtained from the slope of the VTC plot. The gains (A_v) for bulk, bending downward, and bending upward were found to be 25.56 , 7.66 , and 7.5 , respectively. These values show that our inverters surpass previously reported circuitry in flexible silicon platforms;³⁰ the inverters show high gains even at scaled V_{dd} , and hence confirming that they can be used for logic

FIG. 1. Fabrication results. (a) Digital photo of fabricated devices at 2 cm bending radius. (b) Cross-section SEM of fabricated flexible inverters bonded to $125\text{ }\mu\text{m}$ KAPTON sheet. (c) Optical profilometer scan of back surface to confirm surface roughness after back etch process. (d) Top view SEM of fabricated inverters (NMOS: $L_g = 250\text{ nm}$, $W = 350\text{ nm}$ and PMOS: $L_g = 250\text{ nm}$, $W = 450\text{ nm}$). (e) Cross section of Si chip thinning process. (f) Digital picture of flexible devices before laser dicing. (g) Digital picture of devices after dicing.

FIG. 2. Transfer and output characteristics of NMOS and PMOS transistors. (a) Transfer characteristics (I_d - V_g) of NMOS transistor in semi-logarithmic scale for flat, bending downward and bending upward state. (b) Output characteristics (I_d - V_d) of NMOS transistor in linear scale. (c) Transfer characteristics (I_d - V_g) of PMOS transistor in semi-logarithmic scale for flat, bending downward, and bending upward state. and (d) Output characteristics (I_d - V_d) of NMOS transistor in linear scale.

applications due to high noise margins. Finally, the input-low-voltage and input-high-voltage of the inverter were calculated with

$$V_{IL} = V_M - \left(\frac{V_{DD}}{2A_v} \right), \quad (2)$$

$$V_{IH} = V_M + \left(\frac{V_{DD}}{2A_v} \right), \quad (3)$$

where V_{IL} and V_{IH} are the input-low-voltage and input-high-voltage, respectively, and V_M is the switching threshold of the CMOS inverter. The obtained values for bulk sample

FIG. 3. VTC characteristics of flexible inverters in bulk and different bending states inverter AC performance at different bending conditions ($V_{dd} = 1$ V, $V_{in} = 1$ V peak-to-peak, and 1 MHz operation frequency). (a) VTC characteristics of bulk sample before back etch. (b) VTC characteristics of flexible inverters at different bending downward radii. (c) VTC characteristics of fabricated inverters at different bending upward radii. (d) Inverter performance at 2 cm bending downward radius. (e) Inverter performance at 2 cm bending upward radius. (f) Inverter performance after 1500 bending cycles at 2.5 cm bending downward radius.

were 0.393 V and 0.422 V for V_{IL} and V_{IH} , respectively. The values for bending downward were found to be 0.329 V and 0.46 V for V_{IL} and V_{IH} , respectively. Finally, the values in bending upward state were found to be 0.34 V and 0.473 V for V_{IL} and V_{IH} , respectively, for all bending upwards radii. The short range between V_{IL} and V_{IH} and the inverter gains higher than 1 show that the fabricated bulk and flexible inverters will exhibit high noise immunity even at reduced gate lengths and scaled V_{dd} , hence confirming that the devices can operate at different bending radii without compromising performance. It is to be noted that while the channel length is reduced, V_{th} engineering will be required in order to maintain the performance of the inverters. To continue with the characterization, all the inverters were tested at different bending radii under AC signal, the applied signals consist of 1 V for V_{DD} and 1 V peak-to-peak square wave with a 1 MHz frequency for the input port of the inverter. This measurement takes place on a flat surface in order to characterize the circuit under 0 stress condition, and then, the sample is bent to fit different downward and upward bending radii (2 cm). Figs. 3(d)–3(e) shows the results obtained for downward and upward bending states. Finally, the dies are subjected to 1000 and 1500 bending cycles at a 2.5 cm bending radius before testing the devices (Fig. 3(f)–only 1500 cycles shown). The delay parameters (rise time, fall time, rising propagation delay, falling propagation delay, and average propagation delay) were calculated for all different testing configurations. The rise time (t_r) was calculated by obtaining the output crossing from $0.2V_{DD}$ to $0.8V_{DD}$. Fall time (t_f) was calculated by obtaining the time elapsed for the inverter output to fall from $0.8V_{DD}$ to $0.2V_{DD}$. Finally, the average propagation delay of the inverter was calculated with

$$t_{pd} = \frac{t_{pdr} - t_{pdf}}{2}, \quad (4)$$

where t_{pd} is the average propagation delay and t_{pdr} and t_{pdf} are the rising propagation delay and falling propagation delay, respectively. Table I shows the obtained results for rise time, fall time, and average propagation delay at flat, bending downward, and bending upwards states. The propagation delay in the range of “ns” shows the fast switching speed of the fabricated inverters. Increasing the operating voltage can reduce the propagation delay of inverters; however, an increment in V_{DD} will also increase the power

consumption due to the squared relation between V_{DD} and drive current. An alternative to decrease the propagation delay without increasing the power consumption is to decrease the output capacitance of the fabricated devices, for this reason, we designed the inverters with scaled transistor sizes.

In this work, we have shown superior circuit performance in flexible electronics using inorganic substrates in terms of power consumption, gain, and speed when compared to previous reports on organic based devices.^{31–34} The relatively high changes in terms of gain when comparing flat state and bending states can be explained by the reduction in the drive current of the NMOS and PMOS devices and the change in the subthreshold swing due to band splitting and carrier repopulation³⁵ in the silicon channel when strain is applied across the channel of the transistor, since the variation in terms of PMOS and NMOS current is asymmetrical to the strain applied to the channel, the only way to maintain performance of the CMOS inverter would be to design the circuit geometry ratios (W/L) taking into account the variations in hole and electron mobilities and SS caused by specific values of strain applied to the channel of the devices. Since gain is directly related to V_{IL} and V_{IH} changes, the carrier repopulation in the thin silicon channel of the transistor also explains the change in V_{IL} and V_{IH} for downward bending and upward bending. Even though the devices show a reduced gain when they are bent to different radii, it can be seen that the performance is maintained the same in terms of V_M , V_{IL} , and V_{IH} , hence confirming that the devices can still operate as inverters even at extreme bending radii values and reduced V_{DD} voltages. It is to be noted that a comparison with previously reported work²⁶ shows that our reported inverters have similar performance even when driven at V_{DD} values six times smaller, therefore confirming that silicon based inverters can operate in flexible platforms with a decreased power consumption required for wearable and implantable electronics. The flexible substrate has a final thickness of 40 μm , giving us the ability to bend the devices to a minimum-bending radius of 1.5 cm. The fabricated devices show competitive electrical behavior and bendability relying solely on mature micro- and nano-fabrication techniques. Also, it can be seen that very low rise and fall times have been achieved. This shows that the circuitry can be used for high-speed, low power logic applications even when they are driven at a scaled $V_{dd} = 1$ V, being this one of the

TABLE I. Characterization summary for inverters at rigid, flexible, and different bending radii states.

	State	Strain (%)	Rise time (ns)	Fall time (ns)	Average propagation delay (ns)
Bent downward	Rigid	...	31	31	2.33
	Flexible	...	31	31	2.53
	5 cm	0.043	32	32	2.64
	2.5 cm	0.086	31	31	2.23
	2 cm	0.1075	31	31	2.24
	1.5 cm	0.143	32	32	2.17
Bent upward	1 cm	0.215	31	31	2.35
	5 cm	0.043	31	31	2.23
	2.5 cm	0.086	31	31	2.54
	Bent downward 1.5 cm after 1500 cycles	0.143	31	31	2.37

major challenges in circuit design in order to reduce power consumption. Also, the average propagation delay is in the range of 2–3 ns, showing the high performance of the fabricated devices. It is important to note that the fall and rise times are kept approximately equal, which is also a major challenges in the case of CMOS circuitry in order to obtain similar response times from high to low and from low to high states. It is to be noted that in this work, 1.5 cm bending radius is shown as a hard threshold, this happens because when the devices are submitted to bending radii below 1.5 cm, the connections made from the contact pads and the devices through vias start to degenerate and reduce the device performance. However, redesign of through inter-layer dielectric vias solves this problem, and bending radii below 1 cm can be obtained.²

The high performance shown by the state of the art flexible CMOS circuitry depicted in this work gives us a deep understanding of the most logical way to proceed in order to integrate billions of transistors on a flexible platform needed to obtain high computational capabilities. Comparing our work to previous results,^{11,17} the advantages of our method includes: enhanced electrical characteristics, state of the art fabrication with common materials, similar flexibility without the need of external polymeric substrates, high integration densities, no lithographic constraints added, transistor sizes in the range of nm without the need of special processes, most sophisticated set of high- κ /metal gate materials, no thermal budget constraints, competitive chip sizes due to scaled transistor integration, and use of commonly used (100) Si substrates. Future work includes the design, fabrication, and packaging of robust CMOS circuitry that would be able to form completely flexible high-performance CMOS based systems for wearable and implantable electronics.

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