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Enhanced cooling in mono-crystalline ultra-thin silicon by embedded micro-air channels

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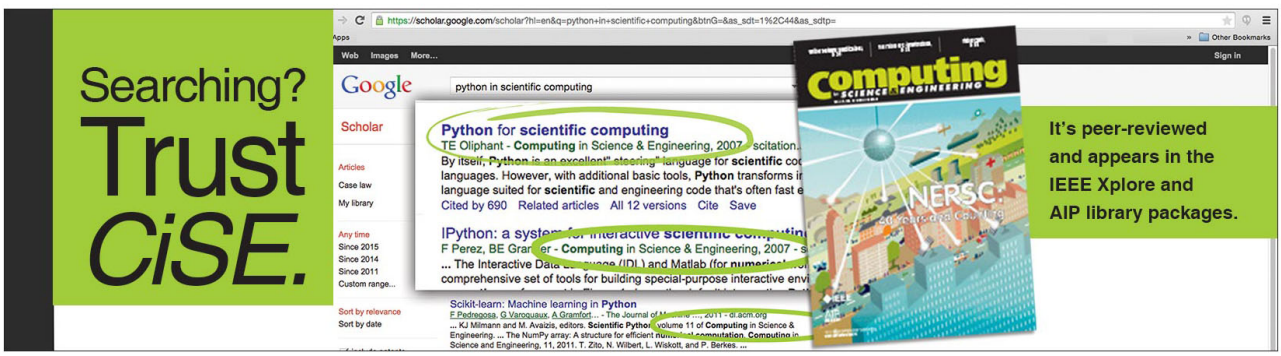

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Enhanced cooling in mono-crystalline ultra-thin silicon by embedded micro-air channels

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In today's digital world, complementary metal oxide semiconductor (CMOS) technology enabled scaling of bulk mono-crystalline silicon (100) based electronics has resulted in their higher performance but with increased dynamic and off-state power consumption. Such trade-off has caused excessive heat generation which eventually drains the charge of battery in portable devices. The traditional solution utilizing off-chip fans and heat sinks used for heat management make the whole system bulky and less mobile. Here we show, an enhanced cooling phenomenon in ultra-thin (>10 μm) mono-crystalline (100) silicon (detached from bulk substrate) by utilizing deterministic pattern of porous network of vertical "through silicon" micro-air channels that offer remarkable heat and weight management for ultra-mobile electronics, in a cost effective way with 20× reduction in substrate weight and a 12% lower maximum temperature at sustained loads. We also show the effectiveness of this event in functional MOS field effect transistors (MOSFETs) with high-κ/metal gate stacks. © *2015 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/).* [http://dx.doi.org/10.1063/1.4938101]

I. INTRODUCTION

Ninety percent of today's electronics are made on low-cost bulk mono-crystalline silicon (100). Scaling of device dimensions has enabled performance enhancement but as a trade-off scaled devices experience higher leakage current induced excessive power consumption in their idle state.[1–7] This also results into higher heat dissipation and eventually lower battery lifetime. With increased demand for ultra-mobile electronics, this rapid power draining acts as one of the main show stoppers. For heat management, traditionally, additional accessories are added into the integrated circuits (ICs) using off-chip fans, for providing forced convection, and heat sinks for providing a large surface area for free-convection and heat radiation but, as a trade-off, making the whole system bulky – counterproductive of the idea of ultra-mobility.[5,8–12] Figure 1 highlights the typical arrangement of key IC packaging in a ceramic ball grid array (CBGA) package, with the primary heat flow path starting from the silicon die to the thermal interface material and heat spreader then to the heat sink and ambient.[13] Yet, an elusive goal is to have an efficient cooling down process which improves the overall reliability of the devices and circuitry – enhancing the performance.[12,14,15] This is because of the multiple dependencies of semiconductors' electrical properties on temperature, starting from underlying electronic structure such as the forbidden energy gap (E_g) range[16] up to the actual current (I_D) flowing in the devices[17–19]; these relations are described by Varshni's empirical expression

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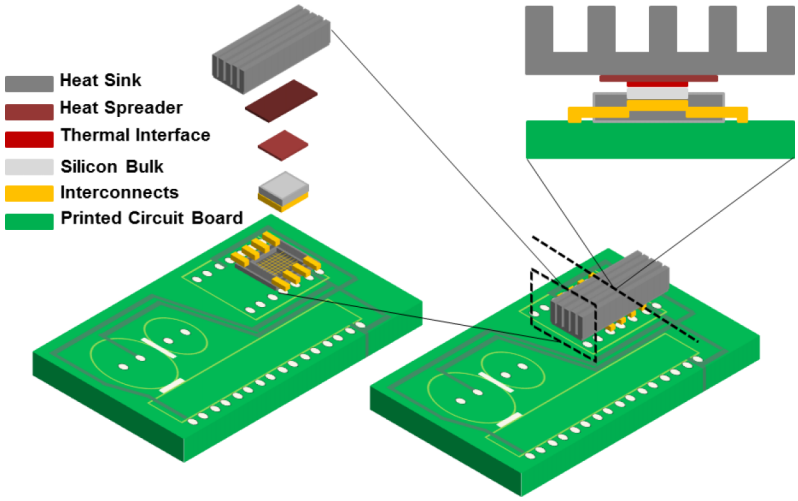

FIG. 1. Typical IC packaging components in a ceramic ball grid array (CBGA) package disassembled (left), assembled (right), showing a cross section of the PCB, chip, and different thermal layers up to the relatively bulky heat sink.

(Equation (1)) and current dependence on temperature (T) (Equation (2)), respectively.

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T + \beta} \tag{1}$$

Where, α and β are material properties,

$$I_D(T) = I_D(0)\, e^{\left(\frac{C}{T}\right)} \tag{2}$$

Where, C is a design parameter.

These thermal effects not only degrade performance but can lead to a thermal runaway causing momentary or permanent device failure,[4,20–23] if the generated heat is not removed promptly and efficiently. This can be a serious challenge for implementing new applications specially related to implantable advanced healthcare electronics.[24,25] Thermal runaway is one of the main challenges that caused Denard's scaling law to be broken in 2005-2007 due to the increased leakage currents with scaling.[26] This is because of the mutual dependency between power and temperature, where a positive feedback loop is created when temperature is raised, leading to increased leakage power consumption which again causes temperature to increase and so on.[27] Performance wise, the dynamic power consumed by a processor is proportional to the generated heat.[28] Dynamic power is related to the clock frequency by Equation (3).

$$P = CV^2 f \tag{3}$$

Where C is the circuit capacitance, V is the designed voltage and f is the operation frequency.

A poor cooling system that cannot dissipate the generated heat corresponding to the designed dynamic power would lead to continuous rising of chip temperature and eventual failure of operation. On the other hand, an efficient cooling system able to dissipate the generated heat fast would allow optimum reliable performance. Extending the discussion further, a cooling system that can go beyond the traditional efficient systems would support higher dynamic power consumption and subsequently a higher clock rate while operating in safe mode.

Flexible thinned silicon has previously been reported as a suitable substrate for flexible electronics.[29–35] Although thinning down silicon leads to a reduced thermal capacitance and faster heating up and cooling down rate, it does not affect the constant load saturation temperature, which is the temperature achieved under constant load at thermal equilibrium. To address a paradox like performance enhancement and higher power consumption with bulky electronics, and inspired by the world's most energy efficient (20W power consumption) computer – human brain's morphology and its cooling architecture through the nasal cavity and fluidic channels,[36,37] we show an equivalent

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substrate structure decorated with an embedded deterministic pattern of porous network of vertical micro-channels for air flow. We further discuss the effect of this transformed structure on heat dissipation through a combination of practical experimentation and theoretical simulations. It is to be noted that in the past, we have used this platform for transforming traditional integrated circuits (ICs) into flexible and semi-transparent ones without compromising the initial high performance, ultra-large-scale-integration density, or imposing extra thermal budget limitations.

II. EXPERIMENTAL SETUP

The origin of the generated heat in electronic circuits is the active device area[38,39] and dense interconnects layers.[40] This is referred to as the chip junction temperature (T_J), which is always higher than the package temperature, related by Equation (4).

$$T_J = T_{ambient} + \left(R_{thermal} x\ P_{package}\right) \tag{4}$$

Where, $R_{thermal}$ and $P_{package}$ is the junction to ambient thermal resistance in °C/W and the power dissipation in the package, respectively. Hence, in our study we focused on the silicon substrate itself, which has the highest temperature in an electronic package and hosts the sensitive computational devices in intimate contact that constitute the circuit. Heating up of the samples in both simulation and practical experiments was done using a heat source (hotplate) from below (similar to the case of 3D integrated ICs) and cooling down was mainly due to free convection throughout, suitable for free form portable electronics for future mobile and internet of things applications. Furthermore, additional experiments were done with heating through current injection in crossbars interconnects until thermal equilibrium is reached for observing the constant load saturation temperature, then cooling down freely (free convection).

A. Fabrication

In the past, on ultra-thin silicon with deterministic pattern of porous network of vertical micro-air channels, we have demonstrated various functioning physical electronics including MIMCAPs,[41,42] MOSCAPs,[43–46] MOSFETs,[47] FinFETs[48,49] (including high temperature study[50]), thermoelectric generators (TEGs),[51] and memristors[52] and have also reported their full performance analysis (both electrical and mechanical)[41–52] and their long term mechanical and electrical reliability and stability.[42,43,49,50,53] In all of those studies we consistently observed no noticeable electrical performance variation due to the ultra-thin silicon. Here we restrict the study to the ultra-thin silicon itself (later in this paper, we extend the discussion to crossbars metallic lines for current injection heat generation/dissipation effects, demonstrate representative functional devices on ultra-thin silicon, and report their performance characteristics and reliability aspects). Figure 2 briefly depicts the main steps for peeling off the ultra-thin silicon with micro-air channels. First, a silicon wafer is oxidized to 300 nm thermal silicon oxide (SiO_2) (Figure 2(a)). Then, standard photolithography is done using ECI 3027 positive photoresist (PR), 200 mJ/cm^2 constant energy dose, and 726 MIF developer to pattern vertical channels in PR (Figure 2(b)). The pattern is formed based on where the chip does (will) not have any devices (this deterministic pattern allows the follow-up vertical channel formation through the passive or STI areas). The patterned PR is used for transferring the same pattern to the thermal oxide using a combination of physical and chemical etching (reactive ion etching-RIE) then deep reactive ion etching (DRIE) of silicon to the desired depth using the Bosch process of successive etching/deposition cycles for smooth side walls (Figure 2(c),2(d)). Afterwards, similar to the spacer formation technique, an atomic layer deposition (ALD) of 50 nm aluminum oxide (Al_2O_3) is deposited at 300 °C followed by a vertical RIE etch leaving only sidewalls protection (Figure 2(e),2(f)). Finally, the sample is put in a XeF_2 reaction chamber for isotropically etching the exposed silicon (available only at the bottom of the vertical channels), releasing an ultra-thin silicon with a deterministic pattern of heat dissipating micro-air channels for enhanced cooling (Figure 2(g)). The last step is not required but for our study we needed a simple vanilla silicon substrate; thus, we immerse the sample in BOE 7:1 for few minutes until Al_2O_3 spacers and thermal oxide are etched

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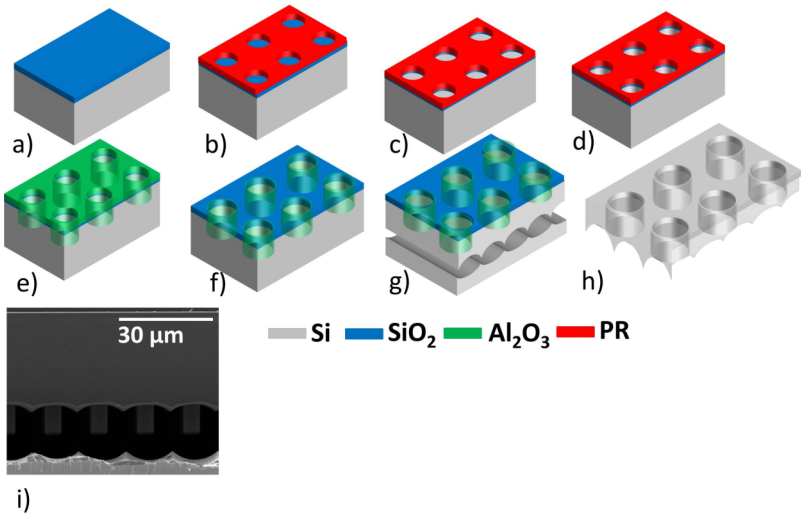

FIG. 2. Fabrication process for ultra-thin flexible silicon with embedded network of micro-air channels: (a) mono-crystalline silicon (100) wafer with 300 nm thermal silicon dioxide, (b) spinning and patterning of positive tone photoresist (PR) coating ECI 3027, (c) etching circular micro-air channels in oxide layer using reactive ion etching (RIE) and PR mask, (d) etching deeper micro-air channels into the silicon substrate using deep reactive ion etching to create the micro-air channels in the substrate, (e) stripping PR and depositing 50 nm of Al_2O_3 using atomic layer deposition for conformal step coverage of sidewalls, (f) highly directional vertical etching of Al_2O_3 using RIE, leaving only sidewall protection (similar to CMOS spacer forming technique), (g) isotropically etching silicon from the bottom of the micro-air channels in a XeF2 etching chamber, releasing a thin silicon bearing micro-air channels and isolating it from the thick silicon bulk, (h) immersing the sample in buffer oxide etching (BOE) bath to strip the thermal SiO_2 and spacer Al_2O_3, and (i) Scanning electron microscopy (SEM) depicting a cross section of the ultra-thin silicon bearing the micro-air cooling channels before BOE bath.

leaving an all silicon channel-bearing thin substrate (Figure 2(h)). It is to be noted that transferring such ultra-thin silicon on another destination substrate for flexible electronics application is analogous to formation of silicon-on-insulator substrate using Smart Cut™ or SIMOX™ technology.

B. Characterization

The characterization was done using an OPTOTHERM InfraSight MI320 (Opto Therm, Inc.) thermal imaging equipment with thermoelectric temperature controller varying the stage temperature for substrate heating up rate measurement. The camera temperature of the thermal imaging equipment was used throughout, since this is more suited than using emissivity tables when lens-to-object distance is less than 2.5 cm. In case of current injection analysis, a Triple Output DC Power Supply (Agilent E3631A, Agilent Technologies) was used to enforce constant voltage while sensing the flowing current.

Table I summarizes the Design of Experiments (DOE) for practical investigations. The released substrate thickness is 30 µm, confirmed by scanning image microscopy (Figure 2(i)). The same thickness was maintained with slight variations (~16%) based on vertical channels pattern (Table I).

C. Simulations

Table II summarizes the design of experiment (DOE) and the targeted outcomes. The simulations are done for silicon samples at an initial temperature of 220°C and ambient 20°C. Applied equations for convective cooling (Equation (5)) and surface to ambient radiation (Equation (6)) are given by:

$$-n.(-k\nabla T) = h.(T_{ambient} - T) \tag{5}$$

Where, h is the heat transfer coefficient of air taken as 30 W/m^{2}K.

$$-n.(-k\nabla T) = \varepsilon\,\sigma\left(T^4_{ambient} - T\right) \tag{6}$$

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TABLE I. Design of experiments (DOE) for practical experimentation.

Sample	Thickness (μm)	Micro-air channel diameter (μm)	Pitch (μm)	Metal lines width (μm)
A	50	5	20	...
B	50	10	20	...
C	50	10	30	...
Bulk substrate	500	...	...	...
Ultra-thin silicon with micro-air channels and metal lines	50	5	20	2
Bulk substrate with metal lines	500	...	...	2

Where, ε is the emissivity of silicon taken as 0.7 and σ is the Stefan Boltzmann constant 56.7 $nJ/m^2\ sK^4$.

All simulations were done on finite element analysis software (COMSOL Multiphysics 4.3). Further optimization of the theoretical model is not essential for our study as the same case is applied for both bulk and ultra-thin silicon with deterministic patterns of vertical channels (transformed silicon), and only the relative improvements are of interest. Figure 3 depicts various ultra-thin silicon substrates with micro-air channels *vs.* bulk silicon down freely from 493K.

III. DISCUSSION

In real-life practice, one would opt for maximum real estate wafer area for building devices. Hence, we focus our study on one of the most important effective channel pattern distributions: 5 μm diameter vertical channels with 20 μm pitch, allowing 15 μm spaces for devices between every two consecutive channels. The percentage of the lost surface area following this pattern is given by:

$$\frac{A_{Channel}}{A_{Unit\ cell}} = \frac{\pi r^2}{A_{Unit\ cell}} = 4.9\,\% \tag{7}$$

Where r is the radius of 2.5 μm of the top lateral area of the channel, and the unit cell is a 20 μm x 20 μm square area. This is absolutely consistent with the International Technology Roadmap for Semiconductors (ITRS) projections showing that shallow vertical channel isolation (STI) would still consume 20% of active chip area even with extreme scaling, depicted in Figure 4.[54] Figure 5 shows the thermal footprint of various devices built on bulk silicon substrate. Large device sizes are depicted to overcome the limitation imposed by the infra-red resolution (10 μm pixels). The devices have an aluminum (Al) metal top electrode which shielded the substrate temperature underneath, as evident from the non-varying room temperature top electrode while the surrounding substrate temperature rises. Hence, we restrict the thermally observed regions to substrate surface area which should have the highest temperature in a chip (junction temperature). The ultra-thin silicon with micro-air channels sample reached thermal equilibrium at a much lower temperature (~6°C less) compared to the

TABLE II. Various simulated micro-air channel distribution patterns.

Sample ID	Substrate thickness (μm)	Micro-air channel density (number/μm^2)	Micro-air channel diameter (μm)
1	500	0	0
2	50	0.0025	10
3	50	0.0011	10
4	50	0.0044	5
5	50	0.0016	5
6	25	0.0025	10
7	25	0.0011	10
8	25	0.0044	5
9	25	0.0016	5

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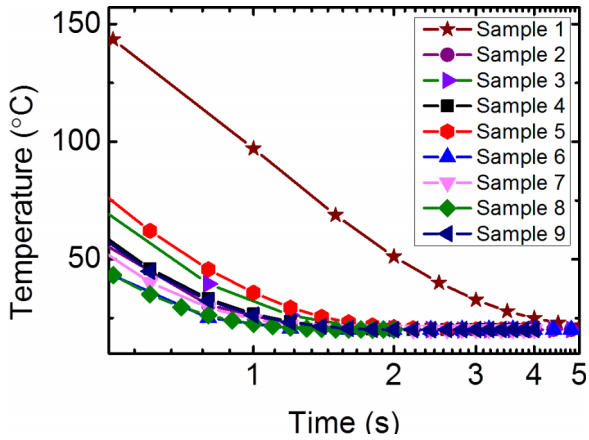

FIG. 3. Simulation results for various ultra-thin silicon substrates with micro-air channels *vs.* bulk silicon, cooling down freely from 493K (plot showing a zoom-in of the last few seconds to highlight the enhanced heat dissipation of the ultra-thin silicon with different size of micro-air channels distributions versus that of the bulk sample).

bulk counterpart (Figure 6(a)). This is explained by the reduced thermal resistance (Equation (8)) of the ultra-thin silicon substrate due to the much reduced length and slightly reduced surface area, since the heating occurs at the bottom of the substrate contacting the hotplate, then, travels upwards through the silicon thickness (10 times longer in bulk), across the cross sectional area (only 5% less in ultra-thin flexible silicon fabric with micro-air channels), resulting in significant reduction in thermal resistance and consequently a lower constant load saturation temperature (depicted in Equation (4)).

$$R_{thermal} = \frac{Length\ (in\ direction\ of\ Heat\ flow)}{Cross-sectional\ Area\ (perpendicular\ to\ the\ heat\ flow)\ x\ Thermal\ Conductivity} \quad (8)$$

However, the ultra-thin silicon with micro-air channels (Figure 6(b)) did not cool down as fast as predicted in simulation results (representative sample depicted in Figure 6(c)) which showed that various vertical channel distribution patterns in ultra-thin silicon cooled down much faster than bulk when both were heated up to 220°C (Figure 3). The discrepancy is due to the fact that real life experiments are more complicated and involve multiple intertwined effects that were simplified in the simulation, namely, in this case it is the effective heat transfer coefficient through the cylindrical micro-channels, which is estimated to be only 10% of the simulated value inside the micro-channels.

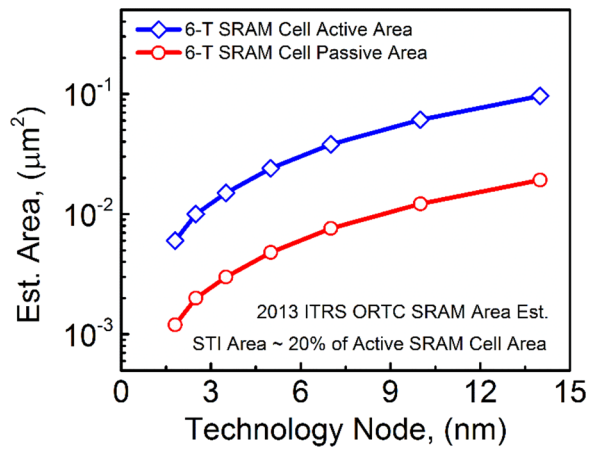

FIG. 4. ITRS projections showing that even with extreme scaling down, 20% of chip area would still be consumed by shallow trench isolation (STI). (List of Nomenclatures: ITRS = International Technology Roadmap for Semiconductors; SRAM = Static Random Access Memory; ORTC = Overall Roadmap Technology Characteristics).

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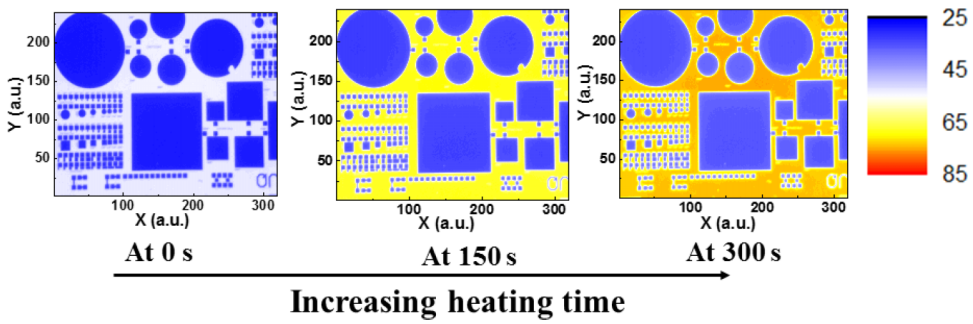

FIG. 5. Thermal mapping of bulk substrate bearing various sizes of devices while heating up showing that devices' metallic top layer shields the substrate active surface heating effect due to their fast cooling rate establishing equilibrium, eve, at elevated temperatures, between dissipated and released thermal energy prohibiting observing surface temperature. Hence, we focus on observing the silicon substrate areas' temperature where there are no devices during heating and cooling experiments.

Still, the simulation results are useful in understanding the direct relationship between substrate structure and the effect on cooling down patterns. There are two factors contributing to the faster cooling of micro-channels bearing silicon simulations: the first is the difference in thickness of the substrates and the second is the presence of the vertical channels. In order to better understand the origin of the different heat dissipation patterns, simulations with two samples having the same thickness with the only difference being the presence of vertical channels were carried out. The results are shown in Figure 6(d). Comparing Figure 6(d) with Figure 6(c), we notice that the improvement in cooling vertical channels and lower thickness is ~80% as the bulk reached ambient in 5 seconds compared to 1 second for ultra-thin silicon (substrate); whereas, when the thickness factor is omitted in Figure 6(d),

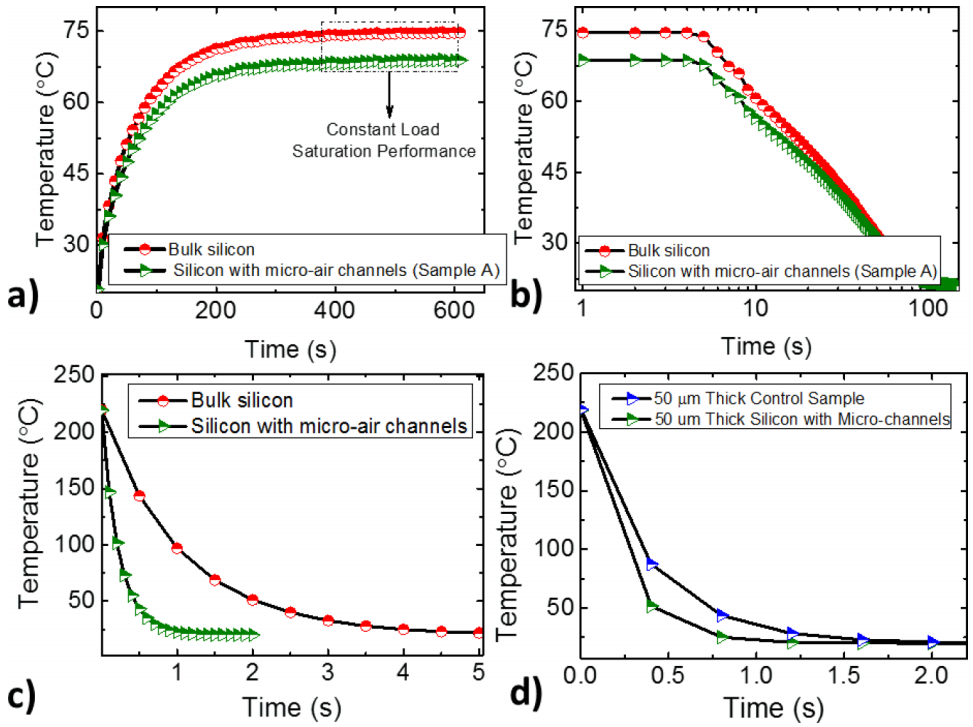

FIG. 6. Heat dissipation in bulk *vs.*ultra-thin silicon substrate with micro-air channels while (a) heating up, (b) cooling down, (c) simulation results for ultra-thin silicon with micro-air channels *vs.* bulk silicon cooling down from 220°C to ambient (20°C), and (d) Simulation results focused on cooling down due to the effect of micro-air channels, to separate the enhancement resulting from thickness variation and that resulting from the presence of the micro-air cooling channels.

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the improvement is reduced to 40%. This can be understood in terms of both factors aforementioned affecting the heat dissipation rates, surface area to volume ratio and the heat capacity of the samples. The higher the surface area to volume ratio (due to presence of micro-air channels), the lower the heat capacity (due to less volume) resulting into the faster cooling down.

Traditional 4" substrate thickness is 500 μm while our ultra-thin silicon substrate with micro-air channel is 30 μm thick with 20% reduction in volume due to the removal of material from the air cooling channels. This results in 20 times reduction in electronics host substrate's weight. Worth mentioning that reducing the substrate thickness adds to reduction in weight advantage but it is an insignificant gain compared to the weight cuts by cutting on external cooling fans and required heat sinks.

Although improvements in a slower heating up rate and faster cooling down rate are interesting, the most important observation from this experiment is the substantial reduction in the constant load saturation temperature for the cooling ultra-thin silicon compared to the bulk silicon (substrate) samples. So far these results show the potential of a more efficient substrate structure that would enable lower operation temperatures and faster cooling rates. Yet, in a modern microprocessor, the actual generated heat is at the active area of the devices and is caused by the flow of current in these areas leading to the highest temperature in an electronic package (the chip junction temperature). Nonetheless, these results can be very useful for further explorations aimed at implementing these new ultra-thin silicon (substrate) with micro-air channel network in a 3D IC structure[55,56] where another substrate beneath heating-up is analogous to the thermal stage used in this experiment.

In order to emulate heat transport in dense interconnects typical in a modern microprocessor, a cross-bar structure of patterned aluminum (Al) lines was utilized. Therefore, further experimentation was done by fabricating similar substrates, skipping the thermal oxide removal, and depositing and patterning a crossbars interconnect architecture of 200 nm thick × 2 μm wide sputtered conductive aluminum for current flow (Figure 7(a)). Current injection was done using Semi-Probe source measurement units (SMUs) connected to a DC Power Supply (Agilent E3631A, Agilent Technologies) and 100 × 100 μm^2 aluminum pads patterned on the substrates.

The experiment was setup such that a bulk sample and a transformed sample of same size and same crossbars pattern are injected with constant input power (constant forced voltage and constant sensed current since electrical resistance is almost constant at low temperature variations). Figure 7(b) shows the most intriguing result in these experiments; that is, the constant load saturation performance due to continuous current injection for the transformed substrate led to a 12% (3°C less) lower temperature than the temperature increase of the bulk substrate. The 2D plots of these results depict the temperature of 5 mm × 5 mm lateral area of bulk and transformed samples *vs.*time under constant injection power for the first 250 sec then cooling down freely (Figure 8). This result shows that the ultra-thin silicon sample has better thermal management structure that the same constant operation

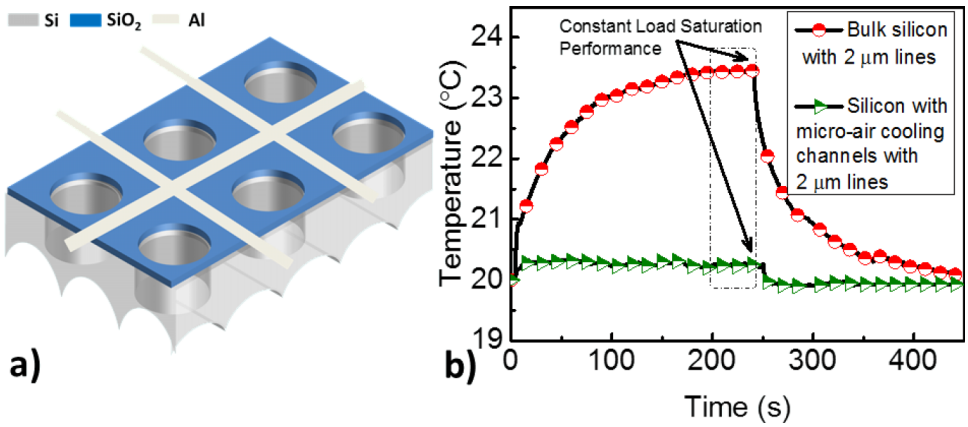

FIG. 7. (a) Schematic of crossbars interconnects on ultra-thin silicon with micro-air channels and (b) constant load saturation performance due to continuous current injection for bulk *vs.* ultra-thin silicon substrate with micro-air channels.

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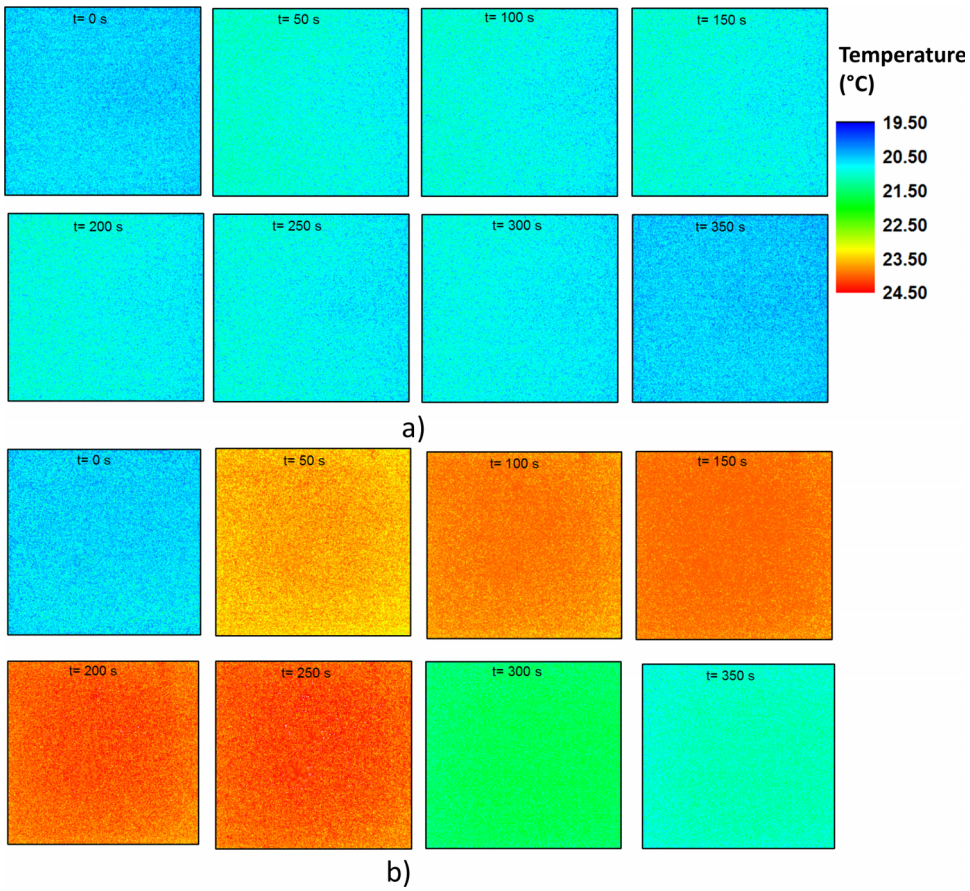

FIG. 8. Surface temperature of (a) ultra-thin silicon with micro-air channels and (b) bulk samples under constant power injection for the first 250 s then cooling down freely.

load leads to a change in temperature of 0.5 °C compared to 3.5 °C in bulk under the same conditions. This is a critical result as it is under sustained heavy workloads that heat dissipation matters, owing to the limitation imposed on maximum power dissipation level by the maximum heat removal rate at static thermal management and constant processing speed.[57]

Common practice in the electronics industry is reporting the performance index "thermal design power (TDP)," which gives a guideline for cooling systems designers about the requirements.[58] The TDP represents the maximum power a central processing unit (CPU) can safely operate at under typical usage, which is always lower (<15%)[58] than the maximum power a central processing unit (CPU) can achieve. Hence, the more efficient the cooling system, the faster it can remove the generated heat due to the higher functionality and the more capable the CPU of working at higher speeds (power) for sustained long durations. However, this comes at the expense of headroom (area), costs, and increased weight associated with the better cooling system (external). Owing to these facts, low-power CPUs are currently designed to fit into the thinner and lighter portable tablets and ultra-books to skip the weight in heat sinks and fans associated with higher performance processors. This will not be the case if an ultra-thin silicon substrate with micro-air channel is used to support high power processors while reducing the requirements imposed on associated external cooling systems. In addition to the better thermal management, the ultra-thin substrate with embedded air-gaps would be suitable for the emerging air-gap STI technology, inherently adding the perks of the technology in terms of superior manufacturability and reliability.[59]

For comprehensibility and feasibility, high-κ (Al_2O_3) metal gate (TaN) stacks were fabricated (Figure 9(a)) using ALD of 10 nm Al_2O_3/ 20 nm TaN followed by 200 nm of sputtered Al for contact. Figure 9(b) shows the structure of a scaled pMOSFET (channel length = 1 μm) fabricated on ultra-thin

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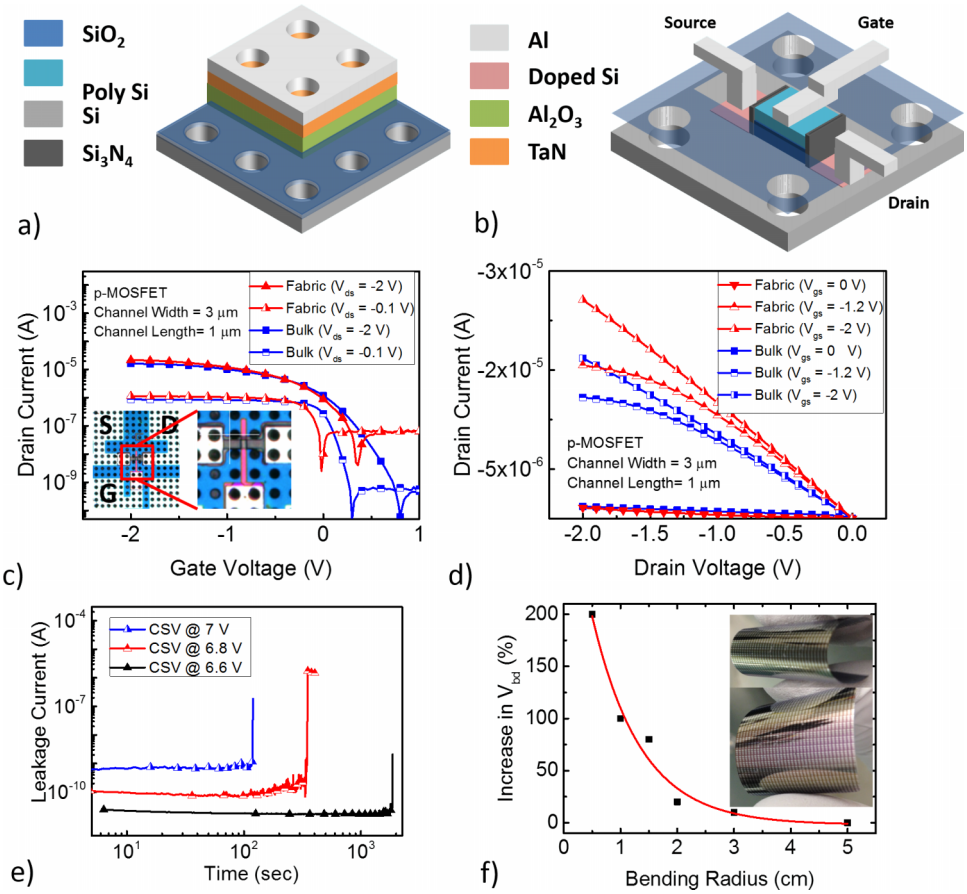

FIG. 9. 3D schematic of pMOSFET devices on ultra-thin silicon with micro-air channels (a) high-κ/metal gate stack encompassing mciro-air channels, (b) scaled pMOSFET with no circular micro-air channels in active areas, (c) transfer characteristics of scaled pMOSFET on bulk and ultra-thin silicon with micro-air channels showing slight increase in on current and a strongly expressed off current increase, inset showing the top view of a flexed MOSFET with channel (pink) between the micro-channels, (d) output characteristics showing slight increase in on currents, (e) reliability time dependent dielectric breakdown (TDDB) of high-κ gate stack devices on silicon with channels under different constant stress voltage (CSV) values, and (f) percentage increase in breakdown voltage of the high-κ gate stacks with lower bending radii for devices encompassing channels in active areas, depicted in (a).

silicon substrate. Figures 9(c) and 9(d) show the transfer and output characteristics, respectively, confirming functionality of pMOSFETs on bulk silicon and ultra-thin silicon with micro-air channels without any significant performance discrepancy. The increase in I_{ON} and I_{OFF} of the flexed devices is attributed to the stress effect of the field oxide on the thin silicon. Figure 9(c), inset shows top view of the fabricated MOSFETs on substrate with a zoom-in on channel passing between micro-air channels. The fabricated devices' active area included the cooling channels, which added to the interfacial defects and trapped charges and affected device performance. Figure 9(e) shows the time-dependent dielectric breakdown (TDDB) analysis for the structures built on ultra-thin flexible silicon fabric (substrate) with embedded network of micro-air channels. The test uses constant stress voltages (CVS) and monitors leakage current versus time to observe the time-to-breakdown (details can be found in Ref. 51). Based on the TDDB and further reliability tests, the MOSCAPs on ultra-thin silicon substrate showed a degradation of 17% in acceptable operational voltage that would pass the 10 years lifetime benchmark, compared to their bulk counterparts. The substrate is also mechanically flexible up to 5 mm bending radius, corresponding to a nominal strain, $\varepsilon_{nominal}$, of 0.3% ($\varepsilon_{nominal} = t/2R$, where t is the substrate thickness and R is the bending radius). Figure 9(f) depicts the relationship between the bending radius at which the stack is stressed and the dielectric breakdown voltage, which shows an asymptotic dependence on bending radius. In-depth mechanical analysis of the gate stacks on

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flexible substrate concludes their suitability for applications where electronic systems are subjected to extended periods of static mechanical stress and minimal dynamic stresses.[43] The detriments of incorporating the micro-air channels into device's structure can be avoided through scaling down of the devices. It is obvious the ultra-thin nature of the substrate makes it prone to structural sensitivity which can be overcome using naturally flexible polymeric encapsulation as well as placement on naturally flexible polymer, fabric, paper, etc.

Finally, it is to be noted that in our prior works we have shown such deterministic pattern of vertical channels based ultra-thin mono-crystalline silicon is highly flexible (bending radius down to 0.5 mm) and semi-transparent (10% transmittance for wide range of color spectrum). These are two additive attributes of ultra-thin flexible silicon substrate with embedded network of micro-air channels for stylish product design.

IV. CONCLUSION

In conclusion, we report on transformation of silicon – a deterministic pattern of porous network of vertical micro-air channel embedded in ultra-thin silicon substrate (derived from bulk mono-crystalline silicon substrate) platform for future electronics that would enable better heat and subsequently weight management due to its inherent structure. The substrate weighs 20× less than typical substrates, does not compromise the ultra-high integration density achievable on silicon, and has micro-air channels that relax the limitation imposed on external cooling systems. This translates into substantial gains in achievable power for CPUs embedded in portable ultra-thin/light weight electronic devices.

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