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Torsion based universal MEMS logic device

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Highlights

- We propose a MEMS logic device, which is capable, of performing INVERTER, AND, NAND, NOR, and OR gates using one physical structure within an operating range of 0-10 volts.
- It can also perform XOR and XNOR with one access inverter using the same structure with different electrical interconnects.
- We use here a non-conducting structure (Polyimide) with patterning of a conductive metal layer to form the gate electrode. This patterned layer allows independent control of mechanical and electrical properties, which provides flexibility and control over the biasing of the electrodes. This allows more gate functions than previously possible using a single basic gate design.
- Theoretical lumped parameter model for torsion based MEMS actuator is also presented.

Abstract. In this work we demonstrate torsion based complementary MEMS logic device, which is capable, of performing INVERTER, AND, NAND, NOR, and OR gates using one physical structure within an operating range of 0-10 volts. It can also perform XOR and XNOR with one access inverter using the same structure with different electrical interconnects. The paper presents modeling, fabrication and experimental calculations of various performance features of the device including lifetime, power consumption and resonance frequency. The fabricated device is 535 μm by 150 μm with a gap of 1.92 μm and a resonant frequency of 6.51 kHz. The device is capable of performing the switching operation with a frequency of 1 kHz.

Keywords: Logic Device; Micromirror; Polyimide

1. Introduction

Zero off-state leakage and abrupt switching behavior [1- 3] of MEMS logic gates provide a potential alternative to the non-zero off-state leakage of CMOS [2], which increases with the downward scaling of transistors. Also an increase in temperature can cause semiconductors to return to their intrinsic performance resulting in uncontrolled behavior of the transistor [4]. Furthermore, CMOS transistors react poorly to ionizing radiation, and hence cannot work in harsh environmental conditions [5, 6]. Mechanical logic gates overcome these hurdles, and hence are important for further exploration.

MEMS/NEMS switches have spiked a large interest in the research community due to their importance in low power digital applications [7-13]. A variety of switches for logic and memory applications have been reported [14-29]. Piezoelectronic transistor and piezoelectrically modulated resistive switching devices have been proposed for very high switching speeds and low power logic and memory applications in [14] and [15] respectively. Mechanical-electrical coupled piezotronic logic operations have been realized in [16] using GaN nanobelt (NB) interface. The technology reported is able to perform multiple logic operations; however it needs an assembly and integration of multiple devices in order to do so. A PZT based switch for low power digital applications is presented in [17]. However, the proposed device is capable of performing a single XOR gate operation only. Dual beam MEMS relays, AlN based, have been reported in [18]. Multiple logic gates, such as XOR/OR/AND within 1 volt, have been realized, however, this has also been achieved by using a combination of the multiple device structures. Furthermore, electrostatically actuated clamped-clamped beams with double-sided electrode configuration for logic operations have been reported in [19]. A combination of these proposed NEMS switches has been shown to perform the NOR/XOR/NAND and an inverter. Similarly, curved cantilevers are proposed in [20] to realize a single stage inverter and buffer.

Complementary MEMS switches that work in a seesaw manner are one of the popular architectures for logic gates since they provide more options to actuate the device and therefore realize more gate operations using a single structure [21-26]. This saves space as well as minimizes delays and most importantly allows for the devices to act as a basic building block for designing complex digital circuits. A four terminal relay technology was published in [22] using the complementary operation of switches to perform logic operations i.e. inverter. Seesaw-relay-based logic and memory circuits have been demonstrated in [23] capable of performing an INVERTER, AND and OR gates. A torsional two layer MEMS logic gate has been reported in [24, 25], which is able to perform NAND and NOR operations using a single device structure. This work is based and will build on the ideas in [24, 25] to realize an all-in-one logic device.

While many MEMS logic gates have been demonstrated, they still lack the flexibility of CMOS in designing a plurality of gates. Differently from above, we here use a partitioned suspended gate electrode, which is mechanically engaged to a non-conducting structure (polyimide). This partitioning of suspended gate electrode allows independent control of mechanical and electrical properties, which provides flexibility and control over the biasing of the electrodes. This allows more gate functions than previously possible using a single basic gate design. Further, our design allows the device to perform both a gate and its complement without the need of an inverter stage. Hence, we report a device that can perform INVERTER, AND, NAND, NOR, and OR gates using one physical structure. It can also perform XOR and XNOR gates with one additional inverter.

2. Operation Mechanism

The torsion based mechanical switch depicted in figure 1, is used to execute all the logic gates. The fixed electrodes underneath the right side of the actuator are made bigger in size as compared to those on the left side. Hence G_L (left gate electrode) has smaller exposed area to input electrodes and will require both

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these inputs electrodes to be active to pull in the left half of the actuator while G_R (right gate electrode) has a larger exposed area and anyone of the input electrodes when active, will pull in the right half of the actuator. When any of these sides snap down there is a contact made between the source and drain on the respective side. These drains are connected to form the output terminal of the logic device. In order to add more flexibility the device is fabricated in such a way that the metal strip at its tip is isolated from the gate electrode itself. This enables the device to transfer a different voltage state than the state on the gate. Hence we can switch a gate operation to its complement by just inverting the input states on the sources on both sides. Table 1 shows the required input states for the device to perform various logic operations. Consider the example for the NOR gate operation, where S_L , S_R , G_L and G_R are hardwired to a specific state as given in table 1. When the input state is (0, 0), we notice that there is a potential difference between G_L and the left side electrodes. Since both of these electrodes are active the device pulls down towards the left side passing the state on S_L (i.e. 1) to the output. Next, when the input is (1, 0) / (0, 1), one electrode on the right side is active, which is enough to pull in the device towards the right side, passing the state on S_R (i.e. 0) to the output. Similarly when the input is (1, 1) the potential difference exists only on the right side hence the device pulls in to the right again and passes the 0 state on S_R to the output. This completes the NOR gate operation.

Figure 1. A 3D schematic of the logic device.

Table 1. States of different electrodes to perform logic operations.
(1=High; 0=Low; V= Applied Voltage switching between 0-1)

Note: S_L , S_R , G_L and G_R would be hardwired to select the gate type in a real application.

	S_L	S_R	G_L	G_R	I_A	I_B	Output
NOR Gate	1	0	1	0	V	V	Out
OR Gate	0	1	1	0	V	V	Out
AND Gate	1	0	0	1	V	V	Out
NAND Gate	0	1	0	1	V	V	Out
Inverter	1	0	1	0	0	V	Out

The proposed device can also perform XOR and XNOR gates with the help of one access inverter as it requires an inverted input signal. Figure 2 shows a schematic demonstrating how the connections should be made to perform these logic gates. Unlike the cases mentioned in table.1, where for a particular gate the biasing type S and G electrodes were hardwired to determine the gate type and there were two inputs like a standard gate, here the gate electrodes (biasing type S) is only hard wired, while the rest are connected to the standard input states. Table 2 shows various input states to perform these gates.

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Figure 2. Schematic showing the electrical interconnects to perform XOR/XNOR gate.

Table 2. States of different electrodes to perform logic operations. (1=High; 0=Low; V_1 = Input voltage 1, V_2 =Input voltage 2, $\text{Inv}(V_1)$ = Inverted V_1).

	S_L	S_R	G_L	G_R	I_A	I_B	Output
XOR Gate	1	0	V_1	$\text{Inv}(V_1)$	V_2		Out
XNOR Gate	0	1	V_1	$\text{Inv}(V_1)$	V_2		Out

One of the gate electrodes is provided with input 1 (V_1) while the other side must be provided with an inverted input 1. The previously input electrodes I_A and I_B are now provided with the same input 2 (V_2). Now whenever the two inputs are the same, the right side will snap down and connect the right side's source and drain while in all the other cases the left side will snap down and connect the left side's source and drain. This explains how XOR/XNOR gates can be performed using the same structure.

3. Modeling

Lumped parameter techniques are used to model the static and dynamic behavior of the device [30]. An expression for electrostatic torque required for the actuation of the micro actuator can be derived as follows. Consider the schematics of figure 3.

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Figure 3. (a) Top view of the device. (b) Schematic side view.

The actuator is composed of an upper plate of length $2a$, width b and thickness t_b . this plate is connected to two flexure beams on the side of length l , thickness t , and width w . These beams act as two springs connected in parallel. There are two different voltages applied on both sides as can be seen in Figure. 2. The length and width of electrodes is different on both sides in order to get the desired output from the logic device. The gate electrode on the left side has a voltage V_{GL} , while each of fixed electrodes on the left side is of width b_l and length $x_4 - x_3$. Similarly the gate electrode on the right side has a voltage V_{GR} while each of fixed electrodes on the right side is of width b_r and length $x_2 - x_1$. The input voltages on these fixed electrodes are V_a and V_b .

Assuming negligible fringing effect, small tilting angle α and infinitely wide plates we can treat the plate and the electrode underneath as two parallel plates. An expression for electrostatic force acting on the right half of the device can be calculated as

$$dF = dF_1 + dF_2 \quad (1)$$

Since there are two electrodes and two different voltages on each side, the force equation also has two terms.

$$dF = \left[\frac{\epsilon b_r (V_{GR} - V_a)^2}{2(d - \alpha x)^2} + \frac{\epsilon b_r (V_{GR} - V_b)^2}{2(d - \alpha x)^2} \right] dx \quad (2)$$

Where ' α ' is the tilt angle and ϵ is the dielectric constant of the gap medium. An expression for electrostatic torque is given by

$$M_R = \int_{x_1}^{x_2} x dF \quad (3)$$

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$$M_R = \varepsilon b_r \left[(V_{GR} - V_a)^2 + (V_{GR} - V_b)^2 \right] \int_{x_1}^{x_2} \frac{x}{2(d - \alpha x)^2} dx$$

(4)

Let

$$V_R = \varepsilon b_r \left[(V_{GR} - V_a)^2 + (V_{GR} - V_b)^2 \right]$$

(5)

We have the equation for the electrostatic torque applied on the right side of torsional actuator as

$$M_R = \frac{V_R}{2\alpha^2} \left[\frac{d}{(d - x_2\alpha)} - \frac{d}{(d - x_1\alpha)} + \ln \left\{ \frac{d - x_2\alpha}{d - x_1\alpha} \right\} \right]$$

(6)

Similarly an equation for the electrostatic torque applied on the left side can be derived as

$$M_L = \frac{V_L}{2\alpha^2} \left[\frac{d}{(d - x_4\alpha)} - \frac{d}{(d - x_3\alpha)} + \ln \left\{ \frac{d - x_4\alpha}{d - x_3\alpha} \right\} \right]$$

(7)

Where

$$V_L = \varepsilon b_l \left[(V_{GL} - V_a)^2 + (V_{GL} - V_b)^2 \right]$$

(8)

Finally the net torque due to electrostatic forces M_{Te} applied on the actuator is given by

$$M_{Te} = M_R - M_L$$

(9)

As a result of this torque applied there is a resilient torque M_{res} induced from the micro flexures given by

$$M_{res} = K_t \alpha$$

(10)

Where K_t is the effective stiffness given by [31]

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$$K_t = \frac{2GJ_p}{l}$$

(11)

Where G is the shear modulus and J_p is given by [30]

$$J_p = \frac{1}{3}wt_b^3 \left(1 - \frac{192t_b}{\pi^5 w} \sum_{n=0}^{\infty} \frac{1}{[2n+1]^5} \tanh \left[\frac{(2n+1)\pi w}{2t_b} \right] \right)$$

(12)

An expression for the pull in voltage can be obtained based on equation (9) and equation (10) [30]. The following equation is simplified to find the pull in for the right side of the micro actuator.

$$V_p = \sqrt{\frac{K_t \theta_s^3}{\epsilon b_r \left[\frac{d}{(d-x_2\alpha)} - \frac{d}{(d-x_1\alpha)} + \ln \left\{ \frac{d-x_2\alpha}{d-x_1\alpha} \right\} \right]}}$$

(13)

where θ_s is the snap down angle. After plugging in the approximate value of θ_s , a relation for pull in voltage V_p can be given by [30]

$$V_p = \sqrt{\frac{0.8275K_t d^3}{2\epsilon b_r x_2^3} (1-\delta^2)^{-0.5} (1+0.6735\delta^{1.931})^{-0.3244}}$$

(14)

Where $\delta = x_1/x_2$

Similarly using the same technique the dynamic model of the micro actuator is given by

$$I\ddot{\alpha} + c\dot{\alpha} + K_t\alpha = M_R - M_L$$

(15)

Where I is the effective moment of inertia and c is the damping coefficient

Next we introduce the following normalized parameters

$$\theta = \frac{\alpha}{\alpha_{\max}}$$

(16)

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$$\alpha_{\max} = \frac{d}{a}$$

(17)

$$\gamma_1 = \frac{x_1}{a}; \gamma_2 = \frac{x_3}{a}$$

(18)

$$\beta_1 = \frac{x_2}{a}; \beta_2 = \frac{x_4}{a}$$

$$(19) \hat{t} = \frac{t}{T}; \quad \mu = \frac{cT}{I}; \quad T = \sqrt{\frac{I}{K_t}}$$

(20)

Using equation (16)-(20) the final normalized equation is given by

$$\ddot{\theta} + \mu\dot{\theta} + \theta = \frac{\eta_1}{\theta^2} \left[\frac{1}{(1-\beta_1\theta)} - \frac{1}{(1-\gamma_1\theta)} + \ln \left(\frac{(1-\beta_1\theta)}{(1-\gamma_1\theta)} \right) \right] - \frac{\eta_2}{\theta^2} \left[\frac{1}{(1-\beta_2\theta)} - \frac{1}{(1-\gamma_2\theta)} + \ln \left(\frac{(1-\beta_2\theta)}{(1-\gamma_2\theta)} \right) \right]$$

(21)

Where

$$\eta_1 = \frac{\epsilon b_r V_R}{2\alpha_{\max}^3 K_t}; \quad \eta_2 = \frac{\epsilon b_l V_L}{2\alpha_{\max}^3 K_t}$$

(22)

Equation (21) can be numerically integrated in time using Runge-Kutta [32] method to find the dynamic behavior of the torsional actuator.

In order to perform the proposed logic functions, it is necessary for the device to operate in such a way that it pulls in towards the left side (smaller electrodes side) only when both the small electrodes are active while in all other cases it should snap down towards the right side (larger electrodes side). In order to verify this functionality of the device we performed mathematical simulations using the model described above as well as finite element FE simulations. Figure 4 explains the state transition and the valid range of tilt angle for the device to operate in the above mentioned fashion. It shows that, when both the left electrodes (smaller) are active the actuator will always pull in to the left side as the actuation torque curve never crosses the resilient torque curve. Similarly when both the electrodes on the right side (larger) are active the actuator will pull in towards the right side. However when one of the electrodes on each side is active the actuator will only pull down to the right within the range of ± 8 milliradians since

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beyond this range the actuation torque and resilient torque curves intersect each other. This range is acceptable, as the maximum tilt angle of the device is 4.38 milliradians, hence validating the design.

Figure 4. Plots of resilient torque and actuation torques under different conditions with an operating voltage of 0-10V.

Similar results are found by performing FE simulations of the device using COMSOL MULTIPHYSICS 4.4 [33]. The materials used for the structure is polyimide PI-2611 with a nominal thickness of $6\mu\text{m}$. A layer of 250 nm of gold is used for the fixed electrodes. The solid mechanics and electrostatic module are coupled to simulate the behavior of the device. A parametric stationary study is used to calculate the pull-in voltage and the differential equations are solved using the direct solver MUMPS, and by using the non-linearity option due to the large displacement generated while the structure is actuated.

Figure 5a shows the pull in results for the case when both electrodes on the right side are active. It can be seen that the device snaps down to the right side as predicted. Also in Figure 5b pull in is demonstrated for the case of one active electrode on each side, and it shows that within this operating range it will always snap down towards the right half. This is a very important result for the proper operation of the device. Similarly Figure 5c shows the device pulling into the left half for the case of both left side electrodes active. The FE simulations validate the results obtained by mathematical model.

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(a)

(b)

Figure 5. Finite-element simulation results. (a) Pull in analysis for the case when both right side electrodes are active. (b) Pull in analysis for the case when one electrode on each side is active. (c) Pull in analysis for the case when both left side electrodes are active.

4. Fabrication

The device is fabricated using a six layer polyimide multi-user fabrication process with polyimide as a structural layer [34]. Using polyimide as a structural layer allows for the patterning of the metal layer to form independent gate electrodes. The dual insulating structure with patterned electrodes allows independent control of mechanical and electrical properties, which in turn provides flexibility and control over the biasing of the electrodes. This greater control of the biasing allows more gate functions than previously possible using a single basic gate design.

Figure 6 presents the process flow diagram of the fabrication process. In the first step 500 nm of oxide is grown thermally in order to insulate the device from the Si substrate shown in Figure 6a. Next step is to lay down the fixed electrodes, source, drain and connecting pads network. A 50nm/250nm of Cr/Au layer is deposited using sputtering and then lifted off forming the desired pattern, Figure 6b. Cr is used for better adhesion of Au layer to SiO₂ layer. A 2 μ m layer of polysilicon is deposited as the sacrificial layer, which determines the operational gap of the device, shown in Figure 6c. This sacrificial layer is there after etched to form anchors and dimples (Figure 6d). Dimples are 850 nm in depth and used to control the points of contact with the substrate. With some dimples connecting source to drain and others to avoid the shorting of the two electrodes. The sacrificial layer is patterned and completely etched through to form anchors exposing the Metal₀ underneath and establishing contact between the connecting pads and the movable gate electrodes. A Cr/Au/Cr layer of 50nm/250nm/50nm is sputtered and then lifted off to form the gate electrodes, Figure 6e. Au layer is sandwiched between the Cr layers for adhesion with both the structural and sacrificial layer. This gate electrode is patterned in such a way that the voltage on the gate is isolated from the connecting dimples at the tip of the torsional actuator. Structural layer comprising of polyimide with a nominal thickness of 6 μ m is deposited next, Figure 6f. Polyimide acts as an insulating structural layer hence enabling independence of the gate electrodes. However the bimorph effect will result in downward curvature if metal is only underneath the structural layer. Therefore another metal layer is deposited on top of the structural layer to balance the stresses and produce a flat device, Figure 6g. A 450 nm layer of Ni was found to give a very slightly downward bend to the

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structure. Finally, after etching of polyimide, which forms the structural layer, the device is released using XeF_2 .

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Figure 6. Process flow cross section of the torsional logic device. (a) SiO₂ deposition, (b) Metal_0 (Cr/Au) deposition, (c) α -Si deposition (d) Dimple and Anchor etch (e) Metal_1 (Cr/Au/Cr) deposition (f) Polyimide deposition (g) Metal_2 (Ni) deposition.

5. Experimental Results

5.1. Device parameters

Figure 7(a) shows the SEM image of the fabricated device. Connecting pads that are used to provide voltage to various input sources as well as collecting outputs are labeled. The voltage from these connecting pads is provided to the gate electrodes through the anchors. Metal layer visible on top of the structural layer is the Ni layer deposited to counteract the bimorph effect. This layer is deposited exactly on top of the Metal_1 layer forming the gate electrodes, which are not visible in the figure due to the polyimide layer on top. It can be seen how these layers can be patterned with the desired accuracy using this fabrication process. It can also be observed how the connecting strip of the metal at the end is isolated from the voltage on the gate electrodes, which allows more flexibility to perform the logic operations.

Figure 7(b) shows the SEM of the bottom electrodes achieved by breaking the suspended polyimide structure on top. It shows how the different sized electrodes are connected to form the two inputs for the logic device. The metal lines around the electrodes are the contact points of various dimples that are spread on the mirror to prevent electrical short circuit of the bottom and top electrodes while switching.

The important device parameters are measured experimentally and shown in Table 3. The pull in voltage for different cases was calculated from the mathematical model, FE simulations as well as from the

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experiment. Table 4 summarizes the results for the pull in voltages and shows that the results are in good agreement with each other.

A slight difference between the FE simulation results for pull in and the experimental results can be observed in Table 4, which is caused due to the simplification in the FE model for ease in computation. Metal layers on top and bottom of the structural layer are integrated into the structural layer, which is different from the actual fabricated device. This simplification causes a difference in the stiffness of the flexure beams and hence in the pull in voltages. However the main aim of these simulations was to predict the pull in location for different cases and verify the desired operation of the device.

(a)

(b)

Figure 7. (a) An SEM image of the fabricated logic device. (b) An SEM image of the fixed electrodes obtained by removing the suspended polyimide structure.

Table 3. Parameters of the logic device.

Length of the device	$2a$	$535 \mu\text{m}$
Width of the device	b	$150 \mu\text{m}$
Electrode location	x_1	$97.5 \mu\text{m}$
Electrode location	x_2	$222.5 \mu\text{m}$
Electrode location	x_3	$-105 \mu\text{m}$
Electrode location	x_4	$-185 \mu\text{m}$
Smaller electrode thickness	b_l	$30 \mu\text{m}$
Larger electrodes thickness	b_r	$42.5 \mu\text{m}$
Flexure beam length	l	$100 \mu\text{m}$
Flexure beam width	w	$15 \mu\text{m}$
Flexure beam thickness	t_b	$5 \mu\text{m}$

Gap	d	1.92 μm
Dimple height		0.86 μm

Table 4. Pull in voltages for different cases of actuations.

Case	Mathematical Model	FEM Simulations	Experiment
Only Smaller electrodes active	8.92 volts	9.5 volts	8.7 volts
Only Larger electrodes active	5.33 volts	5.8 volts	5.2 volts
One electrode on each side is active	8.06 volts	8.3 volts	7.9 volts

5.2. Resonance Frequency Measurement

The resonance frequency of the system was measured using a Laser Doppler Vibrometer (LDV) under vacuum conditions with a damping ratio of 0.02. Simulations predict the natural frequency to be 6.48 kHz, while it is measured to be 6.51 kHz experimentally as shown in Figure 8. It also shows a strong agreement between the experimentally and theoretically calculated natural frequencies of the system.

Figure 8. Frequency response of the logic device.

5.3. Logic Device Operation

Experimental results obtained through oscilloscope measurements show that the device is able to perform all the proposed logic operations within 0-10 volts at a frequency of 1 kHz. Figures 9-13 show the experimental results of the device performing some of the logic operations i.e Inverter, OR, NAND, XOR, and AND gates.

Figure 9. Experimental results for the inverter operation of the proposed logic device. A transition between input (1) $\rightarrow$ output (0) and input (0) $\rightarrow$ output (1) is shown. Scale is 500 μ s/div, 5V/div.

Figure 10. Experimental results for the OR gate operation of the proposed logic device (a) shows the transition between input (1,1) $\rightarrow$ output(1) and input (0,0) $\rightarrow$ output(0) (b) shows the transition between input (1,0)/(0,1) $\rightarrow$ output(1) and input (0,0) $\rightarrow$ output(0).

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Figure 11. Experimental results for the NAND gate operation of the proposed logic device (a) shows the transition between input (1,1) $\rightarrow$ output(0) and input (0,0) $\rightarrow$ output(1) (b) shows the transition between input (1,0)/(0,1) $\rightarrow$ output(1) and input (0,0) $\rightarrow$ output(1).

Figure 12. Experimental results for the XOR gate operation of the proposed logic device (a) shows the transition between input (1,1) $\rightarrow$ output(0) and input (0,0) $\rightarrow$ output(0) (b) shows the transition between input (1,0)/(0,1) $\rightarrow$ output(1) and input (0,0) $\rightarrow$ output(0)

Figure 13. Experimental results for the AND gate operation of the proposed logic device (a) shows the transition between input (1,1) $\rightarrow$ output(1) and input (0,0) $\rightarrow$ output(0) (b) shows the transition between input (1,0)/(0,1) $\rightarrow$ output(0) and input (1,1) $\rightarrow$ output(1).

As commonly done for RF MEMS switches and other logic devices, the electrical and mechanical reliability of the logic device needs to be ascertained. Toward this, several other performance parameters of the device are calculated, which are summarized in Table 5. The switching time is measured using a laser doppler vibrometer where the displacement of the mirror can be studied with respect to time. The contact resistance measured between the Au/Cr contacts has also been measured and tabulated. Mechanical reliability of the device is tested without having the device to pull in and make contact. The device performs mechanically for more than 10^6 switching cycles without any degradation. However when the device is tested with the source and drain electrodes active, the device faced stiction problems and failed due to the degradation of the contacting surfaces, as reported in [35-38]. Several devices were

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tested with the average device lifetime of approximately switching 8000 cycles. Future research for such devices will aim to improve these performance parameters, and specifically, the electrical reliability of the devices.

Table 5. Performance parameters of the logic device.

Power consumption per switching cycle	4.2 pJ
Switching time	8.2 μ sec
Mechanical reliability	$>10^6$
Electrical reliability	~ 8000 cycles
Turn off resistance	$>10^9 \Omega$
Turn on resistance	$\sim 384 \Omega$

Conclusions

This paper presents design, fabrication and characterization of a torsion based universal MEMS logic device. A mathematical model to predict the operation of the device is developed using lumped parameter techniques, which is further validated using FE simulations and experimental data. The device is able to perform all the logic operations i.e. Inverter, AND, NAND, OR and NOR gate with a single structure just by changing the interconnections. It is also able to realize XOR and XNOR gate operation with an access inverter. The logic operations are performed at a frequency of 1 kHz with a minimum operating voltage range of 0-10 volts. Other performance parameters like natural frequency, landing time, power consumption and on/off resistance are also calculated and tabulated. The proposed MEMS logic device has the ability to perform all the logic operations using the same structural unit. Therefore, it forms a basic building block that could be used to realize complex digital operations.

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