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Chemical insight into origin of forming-free resistive random-access memory devices

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We demonstrate the realization of a forming-step free resistive random access memory (RRAM) device using a $\text{HfO}_x/\text{TiO}_x/\text{HfO}_x/\text{TiO}_x$ multilayer structure, as a replacement for the conventional HfO_x -based single layer structure. High-resolution transmission electron microscopy (HRTEM), along with electron energy loss spectroscopy (EELS) analysis has been carried out to identify the distribution and the role played by Ti in the RRAM stack. Our results show that Ti out-diffusion into the HfO_x layer is the chemical cause of forming-free behavior. Moreover, the capability of Ti to change its ionic state in HfO_x eases the reduction-oxidation (redox) reaction, thus lead to the RRAM devices performance improvements. © 2011 American Institute of Physics. [doi:10.1063/1.3645623]

High performance non-volatile memory (NVM) devices require acceptable endurance and stable resistive switching for practical application.¹ Transition metal oxides (TMOs)-based resistive random access memory (RRAM) attracts attention because of their compatibility with the complementary metal-oxide-semiconductor (CMOS) process technology.^{2,3} The formation and rupture of the localized conductive filament with the assistance of reduction-oxidation reaction are a widely accepted explanation for the bipolar resistive switching mechanism.^{4,5} In this mechanism, an initial “forming” stage is needed to breakdown the TMO layer before ultimately a conductive filament is formed through percolation. Such a two-stage mechanism causes the first transition from a high resistance state (HRS) to low resistance state (LRS). For a virgin oxide layer, the voltage required for forming a percolation path (V_{FORM}) can be relatively high, which imposes severe constraint from a circuit design perspective. It would be more desirable if the forming and successive cycle SET voltages (V_{SET}) are similar to each other and relatively low for stable RRAM operation. Moreover, if the V_{FORM} is very high, it is possible that the oxide suffers substantial degradation (trap generation) prior to reaching the compliance current level, which can in turn affect the endurance behavior of the memory device. This is more so for the thicker (5–10 nm) high- κ dielectrics that are currently being investigated for commercial RRAM application. It is, therefore, necessary to develop approaches that can be used to reduce the V_{FORM} and enhance the performance metrics of the RRAM. To address this issue, we have fabricated a multilayer oxide stack comprising an additional buffer layer consisting of TiO_x on top of a HfO_x TMO layer.

This $\text{HfO}_x/\text{TiO}_x/\text{HfO}_x/\text{TiO}_x$ multilayer RRAM shows substantial improvement of SET voltage in cycle-to-cycle uniformity within and between device uniformity. Moreover, electrical characterization shows that these multilayer devices are free from the “forming” process.^{6,7} Here, an in-depth physical analysis to probe the chemical origin for realization of forming-step free RRAM devices has been carried out by advanced nano-scale characterization tools such as transmission electron microscopy (TEM) equipped with electron energy loss spectroscopy (EELS). These findings have potential implications for design of next generation RRAM devices to meet the requirements of commercial product.

The device fabrication process is as follows: a ~20 nm Ti adhesive layer was first deposited on silicon substrates by electron beam evaporation, followed by ~50 nm Pt depositions as a bottom electrode (BE). The multilayer dielectric stack consists of a ~4 nm HfO_x film deposited by reactive sputtering in argon and oxygen ambient, followed by a ~2 nm TiO_x , realized by oxidation of a deposited Ti film in oxygen ambient under the temperature of 450 °C. These two processes were repeated to produce the final four-layer oxide structure of $\text{HfO}_x/\text{TiO}_x/\text{HfO}_x/\text{TiO}_x$. The top electrode (TE) is a ~50 nm TiN, deposited again using reactive sputtering and patterned with lithography and selective dry etching to obtain square-shaped capacitive devices. Figures 1(a) and 1(b) show the cross-sectional TEM micrograph of the four-layer high- κ RRAM stack device. The four distinctive layers of thin films can be observed clearly. The thickness of each oxide layer was measured by averaging over the whole layer using a full-width-half maximum method using layer contrast peak values.⁸ The electrical characterization of the RRAM device was carried out by Keithley 4200 SCS semiconductor parameter analyzer. For all the measurements, the

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FIG. 1. Cross-sectional TEM micrograph of multilayer RRAM devices with (a) low magnification and (b) high magnification. The thickness of the oxide layer was measured by averaging the whole layer based on a full-width-at-half maximum method. It is clear that distinctive multiplayer oxides have been achieved in this work.

voltage was applied to the TiN TE with the Pt BE grounded. The size of the tested device was $100\ \mu\text{m} \times 100\ \mu\text{m}$.

Figure 2(a) shows the typical forming, SET and RESET processes of a single layer HfO_x device followed by five successive cycles. The forming voltage (1.7 V) is larger than the SET voltage (1.1 V), by a margin of 0.6 V. The initial (virgin) state resistance (before forming) is much larger (by two orders of magnitudes) than the HRS resistance after the RESET process. For the forming-step free multilayer RRAM fabricated in this study, the virgin state resistance is similar to the HRS resistance after RESET, as can be clearly inferred from Fig. 2(b). Moreover, the forming voltage (1.5 V) is comparable with the subsequent SET (1.4 V) voltage, which suggests that the *conventional* high voltage forming process is no longer needed for this device. Figure 2(c) shows the SET voltage distribution of the single layer device and multilayer RRAM devices having 500 dc cycles. The distribution of SET voltages in multilayer RRAM devices is more converged as compared with the single layer RRAM devices.

FIG. 2. (Color online) (a) Forming process followed by five successive bipolar switching cycles (i.e., SET/RESET) for single layer HfO_x device. The forming voltage is as large as 1.7 V, which is 0.6 V larger than the SET voltage (1.1 V). The ON/OFF ratio is 10. The inset is the high resolution cross-sectional TEM micrograph of the single layer HfO_x RRAM device. The thickness of the HfO_x layer is 9.70 nm. (b) Initial SET/RESET in the forming-step free multilayer RRAM device. The voltage difference between the first “forming” sweep and the SET voltage is less than 0.1 V. The ON/OFF ratio has been improved from 10 to 100 as compared with the single layer HfO_x device shown in (a). (c) SET voltage distribution comparison of devices between single layer and multilayer RRAM in 500 dc cycles.

FIG. 3. (Color online) EELS results of the fresh multilayer oxide RRAM device showing N K-edge at 401 eV, Ti $L_{2,3}$ -edge at 453 eV, as well as O K-edge at 532 eV. The sharp rise in the Ti $L_{2,3}$ edge can be seen in every oxide layer, indicating Ti has diffused into both HfO_x layers. The point to point distance is 3.0 Å in the EELS line scan. The N K-edge can be clearly observed in the TiN top electrode layer, while no signal was found in the multiple oxides layer. Oxygen atoms counts clearly show up in every oxide layer, while negligible count in the TiN top electrode layer.

To analyze the chemical distribution and origin in the forming-step free multilayer RRAM device, EELS measurements were performed using an FEI Titan TEM, operated at 200 kV in scanning TEM (STEM) mode. The STEM probe size was set to be approximately 1.3 Å in diameter, and the point-to-point distance is 3.0 Å in the line scan. Figure 3 shows the EELS results of the N K-edge, Ti $L_{2,3}$ -edge, as well as the O K-edge of a fresh multilayer RRAM device. The N K-edge can clearly be observed in the TiN TE layer, while no such signal exists in the multiple-layer oxide region. Oxygen signal clearly shows up in every oxide layer, while zero O-count exists in the TiN TE layer. The key observation is that a sharp rise in the Ti $L_{2,3}$ -edge is seen in

FIG. 4. (Color online) ELNES of the TiN top electrode, first HfO_x layer, and second HfO_x layer shown in Fig. 3, respectively. The different Ti states are labeled. The peak shifts towards a lower energy which indicates that a change of Ti ionic state. For the TiN TE, in all the samples, we measured the Ti L_2 -edge onsets at 453 eV. In both HfO_x layers, a shift of the L_2 line to higher energy by 1.0 eV is clearly visible with also an increase in L_3 line intensity. Based on these results, Ti in the HfO_2 has a higher valence state than Ti in the TiN gate.

every oxide layer, indicating that the Ti ions actually diffused/migrated into both the HfO_x layers. Figure 4 illustrates the energy-loss near-edge structure (ELNES) at the TiN TE layer, the first HfO_x layer, and the second HfO_x layer, for the same region shown in Fig. 3. Note that the ELNES is commonly used to elucidate the bonding and localized electronic structure; in this approach, the detailed shape of the EELS edge is studied, as it is a function of the local density of electron states.^{9–11} In general, the $L_{3,2}$ edges of the 3d transition metals contain information about the valence state, coordination, and site symmetry of the central atom. The L_3 edge originates from electron transitions from the inner $2p_{3/2}$ orbitals to empty 3d orbitals of the metal and the L_2 edge originates from $2p_{1/2} \rightarrow 3d$ electron transitions. The relative intensity and energy position of these L_3 and L_2 lines are strongly dependent on the d-band occupancy and, therefore, on the valence state of the transition element. In the case of Ti compounds, the near-edge structures found in the $L_{3,2}$ edges mainly reflect the covalent bonding states resulting from direct and/or indirect interactions between Ti and surrounding atoms. In Fig. 4, for the TiN TE, in all the samples, we measured the Ti L_2 -edge onsets at 453 eV. In both HfO_x layers, a shift of the L_2 line to higher energy by

1.0 eV is clearly visible in Fig. 4 for the EELS spectra taken from the particle edge with also an increase in L_3 line intensity. Based on these results, Ti in the HfO_2 has a higher valence state than Ti in the TiN gate. It also reveals an increase from Ti^{4+} to Ti^{3+} . Ti atoms attract electrons rather than losing electrons. The formation of O vacancies can provide electrons, while Hf vacancies provide holes. Therefore, Ti prefers to diffuse into O vacancy rather than Hf vacancy. This Ti-guided conductive filament growth along O vacancy reduces the randomness of the conductive filament formation and rupture processes, leading to improvement of stability and uniformity of the RRAM device.

In summary, forming-step free RRAM has been achieved using a $\text{HfO}_x/\text{TiO}_x/\text{HfO}_x/\text{TiO}_x$ multilayer structure. Physical analysis using TEM-EELS suggests that Ti diffusion into the HfO_x layer is the chemical origin for of the observed forming-step free behavior.

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