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Low-resistivity C54-TiSi₂ as a sidewall-confinement nanoscale electrode for three-dimensional vertical resistive memory

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A three-dimensional (3D) double-layer HfO₂-based vertical-resistive random access memory (VRRAM) with low-resistivity C54-TiSi₂ as horizontal electrodes is demonstrated using complementary metal-oxide semiconductor processing. The electrical measurements show bipolar resistive switching by using C54-TiSi₂ as electrodes for resistive switching (RS) applications. The statistical analysis exhibits cycle-to-cycle and cell-to-cell stable non-volatile properties with robust endurance (100 cycles) and long term data retention (10⁴ s), suggesting that the ultrathin sidewall of C54-TiSi₂ nanoscale electrodes serve to confine and stabilize the random nature of the conducting nanofilaments. The superior RS characteristics demonstrated here highlight the applicability of C54-TiSi₂ sidewall-confinement nanoscale electrodes to VRRAM. © 2014 AIP Publishing LLC.

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Although the resistive random access memory (RRAM) technology is maturing and getting closer to commercialization, cell density and fabrication cost are still not competitive as compared with 3D vertical NAND flash memories. Hence, there is a need to transform the cell from planar to vertical structures for achieving bit-cost scalable (BiCS) and ultra-high density RRAM.¹ In this way, the concept of vertical-resistive random access memory (VRRAM) has been coined by adapting the state-of-art of NAND Flash memories.² The 3D vertical approach relies in sandwiching the resistive switching (RS) material at the sidewall between a horizontal electrode and a vertical electrode. To achieve that, first, multilayer stacks of alternating materials (metallic/insulating) are sequentially deposited. Second, an etching process through the stacking layers defines vertical hole, and third, the RS layer and vertical electrode are conformally deposited within the vertical hole.

The storage node in VRRAM is redefined by both the etching profile of vertical electrode and the thickness of horizontal electrode, leading to new scaling limits. In vertical direction, the limit is set by the etching process for vertical electrode. For instance, 256 Gbit BiCS flash memory with 32 layers at 45-nm node require etching distortion-free high aspect ratio (HAR: stack height/critical dimension) greater than 60 which is only achievable with the most advanced plasma-etch technology.³ In horizontal direction, the limit for cell array size is mainly determined by the ratio of line resistance of horizontal electrode (R_L) to the resistance of low resistance state (R_{LRS}).⁴ Note that, R_L is defined as the line resistance between the applied voltage source and the evaluated VRRAM cell. For array size of 100 × 100, assuming Cu line at 22-nm technology node, interconnect aspect

ratio of 2, and $R_{LRS} = 10 \text{ K}\Omega$, the resistance ratio (R_L/R_{LRS}) results in a value of 10⁻⁴. In these circumstances, the voltage passing along the line decay by 50% just after 100 columns.⁴ Therefore, the fundamental scaling limit for constructing ultra-high-density VRRAM is horizontal electrodes.

Recently, researches have been searching for the appropriate electrode materials to concurrently meet the requirement of good etchability, low resistivity, and complementary metal-oxide semiconductor (CMOS)-compatibility. Several materials such as W, Pt, Ti, and TiN have been carried out as horizontal electrodes of VRRAM. However, all of them fall in some aspect. W needs reliable etching for pattern generation and improved interface for reliability.⁵ Pt is not CMOS-compatible and is highly expensive.⁶ Ti and TiN have relatively high resistivity, ~70 and ~30 $\mu\Omega\text{-cm}$, respectively.^{7,8} Accordingly, alternative materials for horizontal electrode of VRRAM are urgently needed.

Because of process compatibility, small sheet resistance, and minimal electromigration, metal silicide has been widely used as interconnect material in conventional CMOS industry.⁹ In this regard, C54-TiSi₂ has the lowest resistivity (13 $\mu\Omega\text{-cm}$) among the silicides and can be easily etched by fluorine gases.¹⁰ Since fluorine gases are commonly used to etch SiO₂ by CMOS industry, the HAR mold etching burden is expected to be released. Therefore, C54-TiSi₂ appears as a potential horizontal electrode material to overcome technological hurdles for viable ultra-high density VRRAM.

In this work, as a proof-of-concept, we demonstrate a 3D double-layer VRRAM with C54-TiSi₂ as horizontal electrodes. A statistical analysis of RS endurance and data retention tests in bipolar RS mode was performed to evaluate the retainability and variability of VRRAM. The results of 12 cells, 6 TiSi₂ top layer (TL) and 6 TiSi₂ bottom layer (BL) cells, show temporally (cycle-to-cycle) and spatially (cell-to-cell) stable non-volatile properties. The observed stability

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suggest that the ultrathin sidewalls of C54-TiSi₂ nanoscale electrodes can confine and stabilize the random nature of the RS process by acting as the seeds for conducting nanofilaments (CNF) growth. These RS properties achieved by C54-TiSi₂ as horizontal electrodes showcase its potentials in constructing ultra-high density and reliable 3DVRRAM.

The fabrication process flow of the 3D double-layer HfO₂-based VRRAM test structure is depicted in Figure 1: (a) stacked [SiO₂/Ti (16 nm)/Si (36 nm)] pair layers deposited by sputtering on SiO₂/n⁺-Si substrates, (b) two-step rapid thermal annealing (RTA) in vacuum (0.001 Torr) at ramp rate of 0.1 °C/s first at 600 °C for 15 min and then at 900 °C for 15 min to form C54-TiSi₂, (c) patterning 100-μm-diameter holes by e-beam lithography (EBL) and reactive ion etching (RIE) down to the SiO₂ bottom layer to define the vertical lines, (d) sputtering deposition of RS material/vertical electrode (HfO₂/Pt, 50/50 nm), patterning vias by EBL and RIE down to (e) Si substrates to define horizontal lines, (f) TL, and (g) BL. The dry etching was done by SAMCO RIE 10-NR system with CHF₃/30 sccm/4 Pa/50 W to etch SiO₂ at 20 nm/min and CF₄(O₂)/20(5) sccm/2.6 Pa/50 W to etch C54-TiSi₂ at 30 nm/min. The morphological characterization was conducted by scanning electron microscopy (SEM; JEOL JSM-6700F) and X-ray diffraction (XRD, Rigaku). The current-voltage (I-V) characteristics were measured using Keithley 4200-SC parameter analyzer. During the measurement, the current passing through the VRRAM is recorded when the sweeping voltage was applied to the TiSi₂ layers and the Pt vertical electrode was grounded.

The selection of the optimal silicide was not obvious. At a first glance, NiSi offers low resistivity, low Si consumption and low formation temperature (400–600 °C). However, due to the high boiling points of volatile Ni fluorides, the etching rates to fluorine-based gases are negligible.⁹ In contrast, C54-TiSi₂ can be easily etched by CF₄ due to the low boiling point of TiF₄ (284 °C),¹⁰ while having high Si consumption and high formation temperature (900 °C). Typically, two-step annealing process is conducted for forming C54-TiSi₂, first at 600 °C to form the high-resistivity C49 phase and then up to 900 °C to form the low-resistivity C54 phase. However, different from conventional CMOS technology, in VRRAM, Ti/Si stacked layers are sandwiched between SiO₂ layers, challenging the annealing process due to large thermal budget required to form C54-TiSi₂. At such temperatures, the formation/decomposition of SiO₂ and Si, and

subsequent solid state reactions lead to circular defect features and protrusions arising from tiny pinholes created during the deposition process. To get around this issue, we deposited all the layers at 0.1 Å/s and conducted several annealing approaches to form the C54-TiSi₂. First, we used a quartz-tube furnace with different gases (air, Ar and N₂) and temperature gradients (0.03–0.10 °C/s). However, with this approach, multiple micrometer-sized nearly-circular defects are spread over the whole sample which resulted in colorful interiors when they were observed by optical microscope due to the different degradation levels of the multilayer stacks. According to the reaction schemes proposed by Yong *et al.*,¹¹ the degradation of the film into multiple circular defects at high temperatures can mainly be attributed to the volume expansion caused by the production of SiO(g) by following forming reaction Si(s) + SiO₂(s) → 2SiO(g). The problem was persistent for RTA process with the gas of air, N₂ or O₂. Finally, the circular defects disappeared by applying RTA process under vacuum condition with the ramp rate of 0.1 °C/s.

Cross-sectional SEM images of the stacked (SiO₂/Ti/Si) pair layers before and after RTA process are shown in Figures 2(a) and 2(b), respectively. It can be observed that RTA process leads to the formation of TiSi₂. Figure 2(c) shows the XRD patterns of SiO₂/n⁺-Si substrate without and with stacked (SiO₂/Ti/Si) pair layers (multilayer) after RTA process. For the both samples, the Si (200) peak at 2θ = 33.1° is observed from the Si wafer.¹² In the multilayer sample, we observe three peaks for C54-TiSi₂ corresponding to (311), (004), and (022) planes. Consequently, the complete transformation to C54-TiSi₂ after RTA process is confirmed, guarantying negligible voltage degradation when constructing large cell arrays. Figure 2(d) shows a top-view SEM image of the completed 3D VRRAM devices. “Cell 1”-“Cell 6” indicate the location of VRRAM cells while “Bottom” and “Top” label the accesses to the TiSi₂ TL and BL horizontal electrodes, respectively. Figure 2(e) shows a cross-sectional SEM image of well-defined TiSi₂/HfO₂/Pt top and bottom cells, indicating good etchability to release the HAR mold etching burden during vertical scaling.

Next, we demonstrate the RS characteristics of 12 cells (6 TL and 6 BL cells) by using C54-TiSi₂ as sidewall nanoscale electrodes. The measurement setup is illustrated in Figure 2(f). Before performing the tests, a forming process with a fixed current compliance (CC) of 1 mA is necessary to

FIG. 1. Schematic of the fabrication process flow for 3D double-layer VRRAM test structure. (a) Multilayer deposition. (b) C54-TiSi₂ formation by RTA at 900 °C. (c) Opening vias by dry etch. (d) RS layer and vertical electrode deposition. (e) Horizontal lines definition. Opening vias by dry etching to the TiSi₂ (f) TL and (g) BL.

FIG. 2. Cross-sectional SEM images of the Ti/Si/SiO₂ stacking layers (a) before and (b) after RTA at 900 °C. (c) XRD patterns of the stacked layers (multilayer) and SiO₂/n⁺-Si substrates after RTA annealing at 900 °C. (d) Top-view and (e) cross-sectional false-colored SEM images of 3D VRRAM devices. The scale bar in (d) is 100 μm. (f) Schematic of measurement setup.

switch the cells from an insulating state to a conducting state. Then, an endurance test of 100 sweep cycles and a data retention test for 10⁴ seconds were performed for each cell. The read voltage is 0.1 V for all the measurements. Figure 3(a) shows the I-V curves during the forming process, exhibiting forming voltages of ~8 V and ~12 V for TL and BL cells, respectively. Such difference manifests geometrical dissimilarities between TL and BL cells. According with the tendency of the CNF to form at the corner of the horizontal electrode due to the enhanced electric field,¹³ we found that larger forming voltage of BL cells might be caused by the non-uniform etching profiles. Figure 3(b) shows the I-V characteristics of the first set and reset cycle in bipolar

resistive switching (BRS) mode, revealing similar sharp set and reset events. The set voltage (V_{set}) and reset voltages (V_{reset}) are confined around $+6 \pm 1$ V and -6 ± 1 V, respectively. We have found also threshold resistive switching (TRS) in some cells. TRS offers the possibility of incorporating one-selector-one-resistor (1S1R) cell structure into device to effectively suppress sneak-path problem without adding complexity to fabrication process. We believe that non-equilibrium population of high mobility traps at high electric field can lead to strong electron correlations that eventually result into coexistence of BRS and TRS.¹⁴ However, by fixing the CC at 1 mA, the TRS was not stable for more than one cycle. In order to achieve stable TRS,

FIG. 3. RS characteristics from 6 top (blue) and 6 bottom (red) cells: (a) forming process with CC of 1 mA and (b) I-V bipolar RS curves of the first set-reset cycle of each cell. HRS (squares) and LRS (circles) resistance distribution of Cell 1 TL (blue) and BL (red) obtained from (c) RS endurance test of 100 cycles and (d) data retention test of 10⁴ seconds.

further research should be done to enhance diffusion of oxygen ions by using oxygen-rich electrodes, annealing process, and/or fixing higher CC as it has been pointed by Peng *et al.*¹⁴ Additionally, Figures 3(c) and 3(d) show the high resistance state (HRS) and low resistance state (LRS) resistance distribution of the BL and TL of the Cell 1 (see Figure 2(d)) during the endurance and retention tests, respectively.

FIG. 4. Statistical analysis of the RS characteristics from 6 bottom cells (red) and 6 top cells (blue). (a) LRS and HRS resistance distributions, and (b) voltage set and voltage reset distributions obtained from RS endurance test of 100 cycles, and (c) LRS and HRS resistance distributions during data retention test of 10⁴ seconds.

The endurance reveals a very stable HRS and a slightly variable LRS. Meanwhile, both HRS and LRS are highly stable in the data retention test. Nevertheless, the LRS to HRS resistance ratio is low (~ 10). The high switching voltages and low resistance ratio are ascribed to the incapacity of the circular vertical electrodes to generate an electric field with high local intensity.¹⁵ Future work should be conducted to research sharper vertical electrodes that effectively modulate the RS. However, the high stability of both endurance and retention tests deserve distinctive attention.

To further confirm the variability and retainability, we statistically analyze the endurance and retention performance of 12 cells—6 TL and 6 BL cells. Figures 4(a) and 4(b) show the HRS, LRS, V_{set}, and V_{reset} distributions of endurance test. One can observe that HRS is highly stable for most of the tested cells while showing a small variability from cell-to-cell. On the other hand, LRS of each cell is slightly dispersive during retention test but the variability between cells is less. The most relevant observation from the results of 12 cells is the clear window between HRS and LRS, suggesting a reliable read operation of the proposed VRRAM. Moreover, averaging over all the tested cells, the mean (μ) $\pm$ standard deviation (σ) of V_{set} and V_{reset} are 6.78 ± 0.91 V and -6.36 ± 0.73 V respectively, indicating reasonably well controlled cell-to-cell switching voltages. Figure 4(c) shows HRS and LRS resistance distributions over time under a stress bias of 0.1 V. Most of the cells are highly stable and with no conspicuous decay in both HRS and LRS, showing excellent retainability.

Briefly, the origin of excellent cycle-to-cycle and cell-to-cell switching behavior is analyzed below. In the planar sandwiched metal-insulator-metal RRAM devices, the poor stability can be ascribed to the randomness of the CNFs stemming from the planar electrode. CNFs appear in the form of tree-like structures due to a random dielectric soft breakdown and distribute irregularly in the insulators.¹⁶ Rearrangements of these CNFs can occur for repeated writing/erasing cycles and thus spoil the reversibility and retention of the devices. However, in 3D-VRRAM, the thickness of C54-TiSi₂ is scaled down to nanometer regime that a cross-linking of different CNFs can be vastly reduced, leading to the improvement of the RS characteristics of VRRAM devices.

In summary, we have fabricated a 3D double-layer VRRAM device with C54-TiSi₂ as horizontal nanoscale electrodes using CMOS processing. The ultrathin sidewall of C54-TiSi₂ electrode results in not only reliable switching endurance and data retention of VRRAM but also low cycle-to-cycle and cell-to-cell variability of RS characteristics due to the suppressed rearrangements of the CNFs. It is expected that advancements in 3D-VRRAM technology can be achieved by the implementation of C54-TiSi₂ as sidewall nanoscale electrodes.

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