RF MEMS Fractal Capacitors with High Self Resonant Frequencies

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Abstract—This paper demonstrates RF MEMS fractal capacitors possessing the highest reported self resonant frequencies (SRF) in PolyMUMPS to date. Explicitly, measurement results show SRFs beyond 20GHz. Further, quality factors higher than 4 throughout a band of 1GHz to 15GHz and reaching as high as 28 were achieved. Additional benefits that are readily attainable from implementing fractal capacitors in MEMS are discussed including suppressing residual stress warping, eliminating the need for etching holes, and reducing parasitics. The latter benefits were acquired without any fabrication intervention.

Index Terms—Capacitors, Fractals, Q , RF MEMS, Self Resonant Frequency.

I. INTRODUCTION

The parallel-plate-type capacitor (PPC) is ubiquitously used in integrated circuits and does provide high capacitance densities in general. Nonetheless, capacitors still consume a significant area in most chip designs and enhancing their densities even further is desirable. In MEMS, the capacitance of PPCs is even lower since the sacrificial layer is usually etched away to allow other components to move, and air remains as the dielectric. Further, MEMS PPCs suffer from other problems including plate warping due to residual stresses for example [1, 2].

Fractal capacitors, introduced initially in CMOS [3], are a potential solution for increasing capacitance density; they do not only rely on the typical vertical capacitance present between two different layers, but also benefit from horizontal capacitances given the continuous and fast down-scaling of lateral dimensions in processes. A crude MEMS fractal zipping capacitor/varactor was reported in [4] and some theoretical analysis on fractal capacitors followed in [5].

We calculate the maximum ideal capacitance between two adjacent metals simply using: $C = \epsilon l t / d_{\min}$, where ϵ is the dielectric permittivity, l is the metal length, t is the metal thickness, and $d_{\min}$ is the minimum allowable distance separating the metals as stipulated by the design rules. Ignoring ϵ , t and $d_{\min}$ are usually process specific, unlike l which can be chosen to be any desired length. Hence, it is desirable to choose a process or layers within a process with the highest possible $t/d_{\min}$ ratio. In CMOS and MEMS, the $t/d_{\min}$ ratio, which we name here as the fractal ratio (FR), is typically ‘2’. In MEMS however, it is possible to tailor a

process to obtain a high FR . As an example, the FR in MetalMUMPS [6] can reach up to 10, which is a compelling reason to design fractal capacitors in MEMS.

In this paper, we present fractal capacitors in MEMS and show the many benefits that the fractal geometry bestows upon MEMS capacitors process-wise. Fractal capacitors in CMOS were introduced chiefly to enhance the capacitance density. In MEMS however, they offer several additional advantages from a very different viewpoint as will be shown.

Fig. 1. (a) Moore's Fractal: the 1st iteration all through to the 5th; (b) a complete structure showing a sample 5th order fractal capacitor.

II. CHOSEN FRACTAL GEOMETRY

We restrict the analysis in this paper to fractal capacitors created in a single layer. With that in mind, a variety of shapes exists and a challenge arises in choosing an optimum geometry with respect to for example: maximizing periphery, being process- and design-rule-friendly (sharp angles might not develop/etch well for example at very small dimensions and donut/circular shapes may not be allowed in some processes), ease of routing and connection to measurement pads, etc. Given the aforementioned factors, the fractal shape eventually chosen was Moore's [7] as depicted in Fig. 1(a), where the 1st iteration all through to the 5th are shown. A desirable feature in the Moore's Fractal is that it contains right angles only, which is compatible with all CMOS and MEMS processes.

Fig. 1(b), shows the 5th order Moore's Fractal in black (signal), and a complementary shape in gray (ground) while keeping a specific separation between both (i.e. $d_{\min}$). If no separation existed, both terminals add up to a simple plate. Figs. 2(a), 2(b), and 2(c) show the 3rd, 4th, and 5th order fabricated capacitors in PolyMUMPS [6] respectively. In the following, we explain the benefits that are attained from using fractal capacitors in MEMS, and simultaneously justify the rationale behind choosing the Moore's Fractal.

A. Effective Area Utilization and Symmetry

It is evident from Fig. 2 how very little area is not utilized in this geometry. The efficiency of area utilization here can be further confirmed by comparing it to the Koch Island geometry previously used [3]. Note also how the measurement pads are connected to the capacitor efficiently with minimum wasted area using the single metal layer available. Moreover, most of the other fractal shapes will not enable similar effective area utilization or will require another metal layer to connect the capacitor terminals to measurement pads including the Snowflake, Sierpinski, or Menger Fractals for example [7].

Fig. 2. The fabricated capacitors: (a) 3rd, (b) 4th, and (c) 5th order capacitors; all capacitors are square in shape with a side length of 420μm (excluding pads); note that the etching holes were required in (a) only.

B. Suppressing Residual Stress

PPCs in MEMS suffer from warping due to the residual stresses especially for large plates [8]. The fractal concept suppresses this effect considerably. This is clearly seen in Fig. 2 where no light fringes (shadows) exist and is further confirmed by the optical profiler images shown in Fig. 3(a). For comparison purposes, a PPC was created on the same wafer with the same size and suffered a warping distance of 4.3μm as shown in Fig. 3(b).

C. Eliminating the Need for Etching Holes

Depending on the basic fractal geometrical shape that creates the overall fractal structure, the fractal concept can eliminate the need for etching holes. Since a separation between the terminals already exists, it serves the purpose of etching holes effectively, and simultaneously shortens the etching time significantly. Requiring etching holes or not, and as a basic rule-of-thumb, depends on: (1) the dimension of the basic fractal geometrical shape, and (2) the maximum separation distance allowed between two adjacent holes (or sides) as stipulated by the process rules. If the latter is larger than the former, then etching holes are not required (in PolyMUMPS for example, etching holes must not be more than 30μm apart). If etching holes are not required, then optimizing their number, side-length, and perforation configuration becomes also not

required [9, 10].

Fig. 3. Optical profiler 3D views of the (a) 5th order capacitor and a (b) PP capacitor with the same size. Notice how the warping is clearly visible in (b).

D. Ability to Create Capacitance within a Single Layer

This benefit is important for MEMS designers more than CMOS because CMOS processes possess many metal layers and are always furthest from the substrate. MEMS processes however, often have a single metal layer and is usually the top most layer above the other polysilicon layers. From an RF point of view, polysilicon is lossy and will result in a degraded quality factor (Q). With fractal capacitor design, the capacitance can be created in the single available metal layer for enhanced Q . Further, because the metal layer is usually the top most layer (i.e. furthest from the substrate), both the signal and ground terminals are on the same plane, and there is no longer a need to use the lower layers that are closer to the substrate, the parasitic capacitance is reduced significantly. In turn, the self resonant frequency (SRF) and Q increase.

TABLE I. MEMS FRACTAL CAPACITORS VS. CMOS FRACTAL CAPACITORS

Criterion	MEMS Fractals	CMOS Fractals
Residual Stress	Warping suppressed	N/A
Need for Etching Holes	Eliminated (see Section II.C)	N/A
Variation in the fractal ratio (FR)	Flexible; can tailor a specific process in a typical clean room as desired with relative ease (within usual fabrication limits)	Difficult; restricted to foundry
Removal of oxide (or not)	Possible; results in two distinct capacitance values	Not readily possible
Usually a single metal layer is available	Solves the problem by creating the capacitor using this single layer for enhanced SRF and Q	N/A

Table I summarizes the benefits mentioned and compares them in light of the CMOS process. The purpose of Table I is not to undermine CMOS fractal capacitors; rather, its purpose

is to highlight the benefits that are readily available in the MEMS process if a fractal capacitor is used.

III. EXPERIMENTAL RESULTS & DISCUSSION

For comparison, the 3rd, 4th, and 5th iterations were fabricated in PolyMUMPS as shown in Fig. 2. A single layer that comprises METAL and POLY2 was used to create the capacitor. Hence, the capacitor was 2 μ m thick and 3.35 μ m above the substrate; d_{min} was 2 μ m throughout the structures.

Fig. 4 shows the capacitance (C) and Q measurement results acquired from 1GHz to 10GHz using the Agilent 8363C network analyzer and a Cascade ground-signal-ground coplanar probe. It is evident how the Q is considerably high throughout this frequency range for all three versions.

Sample S_{11} measurements are shown in Fig. 5. In Fig. 5(a), the 5th order capacitor is measured from 1GHz to 10GHz and shows that Q is 28 at 5GHz. In Fig. 5(b) however, it is clearly evident that the SRF for the 3rd order capacitor is beyond 20GHz and that the Q is larger than 4 at 15GHz, which is adequate for some integrated circuit applications [11].

The SRFs for the 4th and 5th order capacitors were 19.795GHz and 15.59GHz respectively, compared to an SRF of 5.5GHz and Q of 8 for the PP capacitor of the same size. To the best of our knowledge, these are the highest SRFs reported for capacitors in PolyMUMPS, and are especially noteworthy given that no fabrication intervention or post-processing was performed. The highest reported SRF in PolyMUMPS previously was 11GHz and Q was not reported at this frequency [12] (see TABLE II).

Fig. 4. Measured (a) C , and (b) Q versus frequency for the three capacitors.

Fig. 5. (a) The S_{11} measurement of the 5th order capacitor at 5GHz with a Q of 28, and (b) the S_{11} measurement of the 3rd order capacitor from 15GHz to 20GHz showing that Q at 15GHz is > 4 and SRF is well beyond 20GHz.

Finally, we note that the benefits acquired herein were attained at the expense of a lower capacitance value compared to the fabricated PPC, which measured 5pF. Hence, we conclude that the capacitance densities are 2.8×10^{-5} F/m² 3.5×10^{-6} F/m² for the PP and 5th order capacitors respectively.

Note however, that most of the 5pF measured in the PPC is a parasitic capacitance coming from the large bottom plate that is separated from the substrate by a 0.6 μ m-thick nitride layer. As such, care should be exercised when comparing both types of capacitors to ensure a fair comparison. Finally, if the presented fractal capacitors were created in two or more layers, then this low C problem would be resolved.

TABLE II. REPRESENTATIVE COMPARATIVE STUDY

Criterion	[1]	[11]	[12]	[13]	This work
SRF (GHz)	4	$< 8^1$	11	$< 8^1$	> 20
Q	4 at 1GHz	23 at 1GHz; 14 at 2GHz	16 at 1GHz	20 at 1GHz; 12 at 2GHz	28 at 5GHz
C (pF) ²	2.5	1.4	1.9	2	0.62 (5 th)

¹ Estimated from the measurements.

² Measured capacitances at 1GHz.

IV. CONCLUSION

A MEMS fractal capacitor has been tested at frequencies as high as 20GHz, which is the highest reported to date in PolyMUMPS. The high frequencies and high quality factors were achieved because the capacitors were suspended 3.35 μ m above the substrate, which reduced parasitics. The aforementioned desirable characteristics were attained at the expense of a reduced capacitance value.

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