Out-of-Plane Strain Effects on Physically Flexible FinFET CMOS

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Abstract—We present a comprehensive electrical performance assessment of hafnium silicate (HfSiO) high-k dielectric and titanium nitride (TiN) metal gate integrated FinFET-based complementary—metal—oxide semiconductor (CMOS) on flexible silicon-on-insulator (SOI). The devices were fabricated using state-of-the-art CMOS technology and then transformed into flexible form by using a CMOS-compatible mask-less deep reactive-ion etching (DRIE) technique. Mechanical out-of-plane stresses (compressive and tensile) were applied along and across the transistor channel lengths through a bending range of 0.5 to 5 cm radii for n-type and p-type FinFETs. Electrical measurements were carried out before and after bending, and all bending measurements were taken in the actual flexed (bent) state to avoid relaxation and stress recovery. Global stress from substrate bending affects the devices in different ways compared to the well-studied uniaxial/biaxial localized strain. The global stress is dependent on the type of channel charge carriers, the orientation of the bending axis, and the physical gate length of the device. We therefore outline useful insights on the design strategies of flexible FinFETs in future free-form electronic applications.

Index Terms—Flexible, CMOS, FinFET, strain.

I. INTRODUCTION

THE Internet of Everything (IoE) envisions the connection of living beings (e.g., humans, plants, animals, and birds) and objects to the cloud, where vital signs, activity rates, and other aspects of daily life can be monitored and analyzed to inform decisions and improve lifestyles. In that sense, IoE devices require close proximity to the human body, fast decision making capability, and low heat dissipation. They must have low power consumption (dynamic and static), high performance, and flexibility. Subthreshold swing (SS) is a critical parameter to this end because it affects the switching speed of a transistor and its dynamic power consumption [1].

The nonplanar 3D architecture of a FinFET device enables low-power operation and further scaling, to cope with Moore’s law [2, 3]. FinFET devices are already commercially available at higher technology nodes (22 and 14 nm). The international technology roadmap for semiconductors (ITRS) predicts a physical gate length requirement of 7 nm by 2025 [4]. Although such state-of-the-art CMOS electronics exhibit unparalleled advantages, they are rigid and bulky making them unsuitable for IoE applications. CMOS electronics thus need to be of freeform—physically flexible and stretchable.

In this work, we applied various mechanical stresses through bending to the flexed FinFET devices to assess their suitability for flexible electronics applications, including IoE and wearable systems, where flexibility and high performance are essential features for components. We quantify and analyze the effect of out-of-plane stress on key performance metrics to provide insights into the integration feasibility of state-of-the-art CMOS devices with new emerging applications.

II. EXPERIMENTAL

We used SOI substrates with a 90 nm SOI layer (100) and a gate first approach. A summary of the main fabrication steps is depicted with a cross-section showing fin internal structure in Fig. 1(a–c), where the inset showing fins orientation. Fig. 1(d–f) show the main flexing steps to transform the rigid substrate into a 50-μm-thick flexible form. We used a Keithley 4200-SCS Semiconductor Characterization System on a manual SemiProbe probe station, as well as curved aluminum surfaces for device characterization (Fig. 1(g)). Bending was done along the fins (i.e., where the bending axis is parallel to the line connecting source and drain) and across the fins (i.e., where the bending axis is perpendicular to the fin length).

III. RESULTS AND DISCUSSION

A. Silicon’s Bending Ability and Limitations

Fracture strength determines the overall mechanical stability of a flexible system. The three-point bending test is widely used to assess the fracture strength of a substrate. For silicon thicknesses below 100 μm, the linear elastic bending beam theory cannot provide an accurate estimation of fracture strength because thin substrates produce a nonlinear deflection-load relationship that is used to estimate fracture strength [8].

In 2015, Liu et al. introduced the large deflection theory of beam to account for this nonlinearity [9]. They offered important insights for theoretical limitations of flexible silicon thinner than 100 μm. Furthermore, based on the application’s required bending radius, the thickness of the flexible silicon substrate must be adjusted such that the applied stress is determined as

\[ \sigma = Y \varepsilon (1) \]

Where \( \sigma \) is the stress in Pascals, \( Y \) is Young’s modulus, and \( \varepsilon \) is the nominal strain, which can be calculated as

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(V_{DD}) into Source (ground) and Gate (ground) terminals, remaining nearly constant as Gate voltage increases until switching occurs. On the other hand, under compressive stress, I_{OFF} is initially higher and gate leakage continues to increase linearly with increasing Gate voltage, indicating conduction through the gate dielectric as current now flows from Gate and Drain into the Source in subthreshold regime and continues even after the transistor is switched ON. This confirms that the effect results from a compromised dielectric integrity caused by compressive stress.

Localized strain enhancement in CMOS transistors has been extensively studied for decades [13], with the assumption that different carriers will respond to stress differently. Wesler et al. used energy band diagrams to explain the different responses to stress with respect to carrier types [14]. For instance, in the suggested SiO_{2}/Si/Si_{0.7}Ge_{0.3} strained structure, a barrier hole well in the valence band corresponds to a surface electron well in the conduction band. The strained silicon surface energy band structure is similar to the bent FinFETs case, where the stress gradient along the silicon thickness due to bending induces a strain effect, rather than the SiGe layer, influencing the effective masses (m*) of charge carriers due to the deformations in the constrained/stretched energy (E) bands \( m^* a \left( \frac{\mu^2}{2K^2} \right)^{-1} \), where \( K \) is proportional to crystal momentum. However, due to band bending in different directions, tensile and compressive strains should form different barrier and surface well structures, depending on carrier type. This affects the transport properties especially at the edges of the channel (or fins) where lateral stress values are relatively higher and extra surface and barrier wells for carriers are likely to form. Oppositely charged free carriers behave differently depending on the bending axis (Fig. 3). Further FEM analysis, as represented by Fig. 5(a), shows a two-dimensional stress distribution in a fin bent across the channel and along the channel. Devices with larger dimensions would show similar stress distribution. The critical point would be for further scaled-down devices where the higher stress regions merge to form different stress patterns, which might stress the whole channel and lead to different behavior. Comparing the two stress profiles, it is clear that bending across the channel leads to different stress distribution than bending along the channel. As can be deduced from the results shown in Fig. 3, electrons are more sensitive to stress when the channel is bent along its length, while holes are more sensitive when the bending axis is perpendicular to the channel length. Because CMOS-based technology utilizes both n- and p-type field-effect transistors (FETs) on the same wafer, the assessed degradation should be the worst-case scenario for both of the two channel types. Furthermore, localized stress due to SiGe source and drain has historically been used to strain the channel and enhance mobility. On the other hand, a dissimilar effect takes place in this study. This is because empirical stress imposed by out-of-plane bending causes a different stress distribution profile and different magnitudes compared to localized stress when both are exposed to same strain values (Fig. 5(b)). The inset in Fig. 5(b) shows the calculation of the displacement required for specific strain and the resulting stress profiles for out-of-plane and in-plane fins, stressed at the same strain values. Using equations (1-2), the stress regime for 0.5 to 5 cm bending radii is 80 to 800 MPa, corresponding to an intermediate stress range relatively lower than that used in strained silicon to engineer mobility enhancements [15]. Still there were cases of mobility enhancements for long-channel devices flexed along the channel, but due to the complexity of the testing setup and sources of variation while contacting the devices, the conclusion would be an anomaly within ±5% for short-channel devices. Other key switching properties are summarized in Table I for short-channel FinFETs bent at ±5 cm bending radius.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Method</th>
<th>% change</th>
</tr>
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<tbody>
<tr>
<td>(SS)</td>
<td>min(\Delta V_{GS}/log (I_{DSL}/I_{DS2}))</td>
<td>~10%</td>
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<tr>
<td>V_{TH}</td>
<td>I_{DSL} - \gamma m - V_{GS} - max \gamma m</td>
<td>~10%</td>
</tr>
<tr>
<td>DIBL</td>
<td>\left( \frac{V_{TH,sat} - V_{TH,lin}}{V_{DD} - V_{DS,low}} \right)</td>
<td>±50%</td>
</tr>
<tr>
<td>\gamma m, max</td>
<td>\frac{\partial I_{DS}}{\partial V_{GS}}</td>
<td>~40%</td>
</tr>
<tr>
<td>I_{ON}/I_{OFF} Ratio</td>
<td>\frac{I_{GS} @ V_{DS} = V_{GS} = V_{DD}} {I_{OFF} @ V_{DS} = V_{DD}, V_{GS} = 0 V}</td>
<td>~33%</td>
</tr>
</tbody>
</table>

The large variation in the drain-induced barrier lowering (DIBL) implies that the devices suffered from significant threshold voltage (V_{TH}) shifts when functioning in the saturation regime. An increment under compressive stress implies that the device suffers higher leakage currents due to a relatively larger reduction in V_{TH}. A decrease in DIBL under tensile stress would lead to a device with relatively larger V_{TH} than designed, and, consequently, lower overdrive voltage (V_{DD} - V_{TH}, where V_{DD} is the supply voltage) and on-state currents (I_{on}). The decrease in the peak transconductance (\gamma m) would degrade the performance of a transistor device while operating as an amplifier, because the gain of an amplifier is proportional to the transconductance of the device. Ideally, ICs are designed to tolerate 10% deviation in circuit parameters. Therefore, for anomalies greater than 10%, serious considerations are essential when integrating such high-performance devices in flexible ICs that are intended to function properly under various bending conditions. This can be mitigated by redundant compensation elements to adjust the parameters. Current design for yield in deep-submicron technologies already uses similar techniques to comply with 3\sigma and 6\sigma standards (\sigma measures variability), accommodating process variations for extremely scaled emerging nodes. For instance, adding a backup transistor connected in parallel when needed to enhance the circuit current as the original transistor experiences increased V_{TH} and lower current. The observed trend for increased gate leakage with bending can be utilized to sense the leakage current and determine the corresponding parameter deviation, allowing us to make dynamic decisions to engage added components and correct
the deviation effect.

To extract the effective mobility \( (\mu_{eff}) \), we use:

\[
\mu_{eff} = \frac{g_d}{W Q_n} \quad (4)
\]

Where \( g_d \) is the drain conductance, \( Q_n \) is the mobile charge density in the channel, and \( W \) is the channel width.

\[\text{Fig. 2. Illustrations on changes in fin dimensions (a), and FEM simulations for Von Mises stress distribution (b).}\]

Fig. 6 depicts the extracted effective mobility values versus \( L_G \) for tensile and compressive bent n- and p-type FinFETs. Conclusively, FinFETs with longer \( L_G \) exhibited higher deviations from the unbent benchmark, for both majority carrier and applied stress types. For instance, a representative n-type FinFET showed a deviation of 13% for an \( L_G \) of 10 \( \mu \)m, compared to a 2.3% deviation for \( L_G \) of 110 nm. Similarly, a representative p-type FinFET had a 90% deviation for \( L_G \) of 10 \( \mu \)m and 2.7% deviation for \( L_G \) of 250 nm. Although the long-channel p-type FinFET exhibited a 90% deviation in its effective mobility, their functionality is still attested as a switch, as evidenced in Fig. 6(c). Under both applied stress types, the on-to-off current ratio \( (I_{ON}/I_{OFF}) \) was about \( 10^3 \) with low gate leakage.

In ultra-large scale integration (ULSI), the flowing drain current in the on-state \( (I_{ON}) \) and the off-state \( (I_{OFF}) \) are critical properties of every device. Depending on the magnitudes of \( I_{ON}, V_{DD} \), and gate capacitance \( (C_g \approx \text{oxide capacitance} (C_{ox})) \), the intrinsic delay \( (t_d) \) of the device is determined as \( t_d = C V_{DD}/I_{ON} \). Fig. 7(a) shows the variation of the gate delay with the \( I_{ON}/I_{OFF} \) ratio for a representative p-type FinFET device. The higher the \( I_{ON} \), the faster the circuit and the total capacitance of the circuit, including parasitic, is proportional to the time constant \( (\tau) \), which affects the speed at which the circuit can operate.

The ultimate goal of strain engineering is to increase \( I_{ON} \) through mobility enhancements. A FET current is given by:

\[
I_D = \frac{W C_{ox} \mu_{eff}}{2L} \left[ V_{DS} (V_{GS} - V_{TH}) - \frac{V_{DS}^2}{2} \right] \quad (5)
\]

\( I_{ON} \) corresponds to the saturation current \( (I_{SAT}) \) when \( V_{DS} \geq V_{GS} - V_{TH} \) and is approximately (discarding short channel modulation effect) given as:

\[
I_{ON} = \frac{W C_{ox} \mu_{eff}}{2L} (V_{GS} - V_{TH})^2 \quad (6)
\]

For a representative short-channel p-type FinFET \( (L_G < 250 \text{ nm}) \), the change in \( I_{ON} \) is less than 1% under both tensile (1.5 cm bending radius) and compressive stress (–3 cm bending radius). This is justified by the insignificant deviations in \( \mu_{eff} \) and \( V_{TH} \) while other parameters are physical.

Even for a long-channel p-type FinFET device \( (L_G = 10 \text{ \mu m}) \)—where the change in calculated \( \mu_{eff} \) is was about 90%—the changes in \( I_{SAT} \) were –2.4% for tensile stress and –1.5% for compressive stress (both at 2.25 cm bending radius), at \( V_{DS} = V_{GS} = -1.5 \text{ V} \). The extreme variation in \( \mu_{eff} \) did not translate into current variation—although the change in \( V_{TH} \) while operating in the saturation regime (extracted using the Ghibaudo method for short-channel devices, i.e. the intercept
with $V_{GS}$ axis from $I_{DS}$/$V_{Gsat}$ vs. $V_{GS}$ plot [16]) is less than 8% in worst-case compressive stress, and less than 1% for tensile stress (at 2.25 cm bending radii).

Hence the calculated mobilities do not reflect actual degradation, which is attributed to the susceptibility of the measurement used for mobility calculations to noise, namely the strong dependence of mobility on $g_s$ which is measured at very low drain voltages (between 25 and 50 mV).

This means that in a battery-operated IoT system, where the device is in standby mode most of the time and leakage power dominates, the useful time before a re-charge would significantly shortened. Furthermore, the effect is not direct due to the existing positive feedback loop between flowing current and temperature. The higher currents increase the temperature. The relation between the temperature and the semiconductor band gap is given by the Varshni’s equation:

$$E_g(T) = E_g(0) - \frac{T^2}{T-\beta}$$

(7)

Where $E_g$ is the band gap in eV, $T$ is the temperature, and $\beta$ is a material property. This in turn reduces the $V_{TH}$ and consequently, increases the current further. This feedback loop is a common cause of thermal runaway failures in ICs. Therefore, the increment in $I_{OFF}$ can yield more sever effects and requires closer circuit level studies to prevent the potential for eventual failures during the useful lifetime of a system.

At the device level, still no observable degradation in switching behavior under various bending conditions is present. The gate leakage is 1000× less than the drain currents, i.e. a minute increase in leakage will not significantly affect $I_{ON}$, preserving functionality.

C. Residual Stress vs. Effective Stress

In microcrystalline silicon transistors, Dong et al. showed...
the effect of bending of flexible TFTs [19]. All measurements were taken in the flat position after the sample had been exposed to various bending stress types and various durations. We anticipate this work to be an important milestone in assessing out-of-plane stress effects on transistor characteristics. However, the study was focused on residual stress rather than real-time actual stress measurements.

We have presented a comprehensive analysis on varying flexed (bent) states of flexible high-performance FinFET CMOS. We have shown this reduces stress recovery when devices are re-flattened. Nonetheless, due to the sensitivity of the measurements, an extra source of variation (i.e., contact resistance) is added. As previously mentioned, the outlined percentage variations are ultimately useful for the actual systems applications, whether it is through flexible ICs for the internet of things (IoT), IoE, or wearable electronics. The results show that most variations are restricted to ±10%, which is similar to the process variations range in deep-submicron technologies where possible mitigation solutions are already practiced; however, compromised gate dielectrics introduce new reliability concerns for devices functioning in the bent state. Moreover, we provide insight into the degree of variation in device characteristics when they are bent, which complements previous work and shows that variations can be

IV. CONCLUSION

We have presented a comprehensive analysis on varying flexed (bent) states of flexible high-performance FinFET CMOS. We have shown this reduces stress recovery when devices are re-flattened. Nonetheless, due to the sensitivity of the measurements, an extra source of variation (i.e., contact resistance) is added. As previously mentioned, the outlined percentage variations are ultimately useful for the actual systems applications, whether it is through flexible ICs for the internet of things (IoT), IoE, or wearable electronics. The results show that most variations are restricted to ±10%, which is similar to the process variations range in deep-submicron technologies where possible mitigation solutions are already practiced; however, compromised gate dielectrics introduce new reliability concerns for devices functioning in the bent state. Moreover, we provide insight into the degree of variation in device characteristics when they are bent, which complements previous work and shows that variations can be
mitigated to render the devices suitable for performing while bent as well as when flattened. This work presents the possibility of adding the flexing ability to industry-grade FinFETs without sacrificing functionality and highlights the various effects that out-of-plane bending has on these devices.


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