Design and Analysis of Delayed Chip Slope Modulation in Optical Wireless Communication

Ki-Hong Park, Member, IEEE, and Mohamed-Slim Alouini, Fellow, IEEE

Abstract

In this letter, we propose a novel slope-based binary modulation called delayed chip slope modulation (DCSM) and develop a chip-based hard-decision receiver to demodulate the resulting signal, detect the chip sequence, and decode the input bit sequence. Shorter duration of chips than bit duration are used to represent the change of state in an amplitude level according to consecutive bit information and to exploit the trade-off between bandwidth and power efficiency. We analyze the power spectral density and error rate performance of the proposed DCSM. We show from numerical results that the DCSM scheme can exploit spectrum density more efficiently than the reference schemes while providing an error rate performance comparable to conventional modulation schemes.

I. INTRODUCTION

The development of solid-state lighting such light-emitting diode (LED) and laser diode (LD) is currently transforming traditional lighting infrastructure. Visible light communication (VLC) leverages inherent benefits of lighting infrastructure to support data transmission via lighting, while still being used for illumination. As such, these optical wireless communication (OWC) systems are being considered as an alternative to traditional radio frequency (RF) communication in free space/indoor and even underwater environments [1], [2]. In this context, baseband modulation schemes such as on-off keying (OOK) and pulse position modulation (PPM) have been recently revisited for the purpose of these applications.

For instance, the rectangular pulse-based pulse modulation schemes above have been proposed generally. On the other hand, pulse dual slope modulation (PDSM) was proposed by using a

K.-H. Park and M.-S. Alouini are with the Electrical Engineering Program, Computer, Electrical, Mathematical Sciences and Engineering Division, King Abdullah University of Science and Technology (KAUST), Thuwal, Makkah Province, Kingdom of Saudi Arabia (Email: {kihong.park; slim.alouini}@kaust.edu.sa).
constant slope pulse instead of a rectangular pulse [3], [4]. It is stated in [4] that this type of modulation can provide better spectral efficiency thanks to the triangular pulse shape than that of binary PPM (2PPM). However, the inherent correlated nature of two binary signals in PDSM severely degrades the error rate performance [5].

In this letter, we propose a novel binary modulation scheme, called delayed chip slope modulation (DCSM), by exploiting the advantage in power spectral density (PSD) of slope-based modulation, while maintaining an error probability comparable to those of rectangular pulse-based modulation schemes. In order to improve the power efficiency of the signal, the duration of pulse duration is reduced compared to the previous schemes and as such the slope in pulse becomes steeper. Delayed encoding enables to remain good PSD of the proposed DCSM despite shorter pulse duration. We also develop a receiver structure based on a zeroforcing hard decision detector. We analyze and evaluate the PSD and error probability of DCSM compared with the existing modulation schemes.

The remainder of this paper is organized as follows. Section II describes the system model and the mode of operation for the proposed DCSM. The PSD and error rate analysis is given in Section III. Numerical results in Section IV shows the superiority of the proposed DCSM. Finally, a brief conclusion is given in Section V.

II. SYSTEM DESCRIPTION

We consider intensity-modulation (IM) and direct-detection (DD) which are typically used in optical wireless communications because of their simplicity of implementation. At the transmitter, the electric current signal is converted to the intensity signal, \( x(t) \). Since the physical quantity of the amplitude in the optical signal is an optical power, \( x(t) \) should be nonnegative, i.e., \( x(t) \geq 0 \). The average optical power is constrained on

\[
\lim_{T \to \infty} \frac{1}{2T} \int_{-T}^{T} x(t) dt \leq \frac{P}{2},
\]

where \( P \) is an average power limit and \( T \) is the symbol duration which means the symbol rate \( R_s = 1/T \). For analysis, we assume an additive white Gaussian noise (AWGN) channel where one-shot received signal is \( y(t) = x(t) + n(t) \), where \( n(t) \) is an AWGN with zero mean and variance \( \frac{N_0}{2} \).
TABLE I. STATE TRANSITION OF TRANSMIT SIGNAL

<table>
<thead>
<tr>
<th>level at beginning</th>
<th>$b_k = 1$</th>
<th>$b_k = 0$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Positive slope transition: $g_p(t)$</td>
<td>Remain 0</td>
</tr>
<tr>
<td>$+\frac{N_c}{2}P$</td>
<td>Negative slope transition: $g_n(t)$</td>
<td>Remain $+\frac{N_c}{2}P$</td>
</tr>
</tbody>
</table>

A. Delayed Chip Slope Modulation

We observed from BER and PSD comparison that the previous slope-based modulation cannot provide reasonable advantage over conventional methods [5]. However, it is obvious that the slope-based modulation has the potential to improve the spectral efficiency since it reduces high frequency component and makes the PSD peaky. On the other hand, it should not make significant correlation between transmit signals of binary inputs to guarantee the error rate performance. We here develop a novel slope-based modulation to resolve these challenges.

The transmit signal function of the proposed DCSM scheme is shown in Table I. When $b_k = 1$ is sent, the transition due to positive or negative slope occurs compared to the amplitude level at the beginning. For a negative slope transition, we utilize the transmit signal

$$g_n(t) = \frac{N_c}{2} g(t; 2T/N_c), \quad 0 \leq t \leq \frac{2(N_c - 1)T}{N_c}$$

(2)

and, for a positive slope transition, we use $g_p(t) = g_n(2(N_c - 1)T/N_c - t)$, where we denote the number of chips used for the transmission of bit 0 and 1 as $N_c$ and we define a triangular pulse as

$$g(t; t_0) = \begin{cases} 
-P\frac{t_0}{t_0} + P, & 0 \leq t \leq t_0 \\
0, & \text{otherwise.}
\end{cases}$$

(3)

On the other hand, when $b_k = 0$ is sent, the amplitude level remains unchanged. When the amplitude level at the beginning is $\frac{N_cP}{2}$ and $b_k = 0$ is sent, the transmit signal is given by

$$x(t) = \frac{N_cP}{2} p(t; 2T/N_c),$$

where we define a rectangular pulse as $p(t; t_0) = P\text{rect}\left(\frac{t-t_0/2}{t_0}\right)$ and $\text{rect}(t/t_0)$ is the rectangular pulse function defined as $\text{rect}(t/t_0) = 1$ for $-\frac{t_0}{2} \leq t \leq \frac{t_0}{2}$ and, otherwise, $\text{rect}(t/t_0) = 0$. When the amplitude level at the beginning is 0 and $b_k = 0$ is sent, it remains zero for $2T/N_c$ duration. We note that, for each bit, we use different duration of transmit signal to improve the power efficiency and match the amplitude levels between transmission of different bits. As such, the chip pulse duration is reduced to $2T/N_c$ compared to the duration
of $T$ in OOK and PDSM and the amplitude level $N_c P/2$ is higher than them. This is expected to make our proposed scheme much better in BER than conventional PDSM scheme. We note that $N_c$ is the trade-off factor adjusting the required bandwidth and power efficiency. The bit durations for $b_k = 1$ and 0 are set to $2(N_c - 1)T/N_c$ and $2T/N_c$ to support the same data rate $1/T$. The amplitude level at maximum in the transmit signal is $3P/N_c$ under average optical power constraint in (1). In Fig. 1(a) and (b), we illustrate the example of transmit signal by applying the DCSM scheme with $N_c = 3$ and 4 compared with conventional OOK scheme in Fig. 1(d). We first expect that this transmit signal can have narrow spectral density since the positive and negative continuous slope transition compensate for very steep transition which can be observed in PDSM and rectangular pulse signals. Secondly, it is viewed in Fig. 1(c) as the OOK signal of chip sequence using a triangular pulse, i.e.,

$$s(t) = \sum_{k=-\infty}^{\infty} c_k g_t(t - kT_c),$$

(4)

where each binary chip is modulated into the triangular pulse of duration $2(N_c - 1)T/N_c$ which is given by

$$g_t(t) = \frac{N_c P}{2} \left( g(t - T_c; T_c) + g(T_c - t; T_c) \right)$$

(5)

for every chip duration $T_c = 2T/N_c$.\footnote{We note that this binary chip sequence is highly related to original bit sequence.}

With this structural observation based on chip sequence, we can design a receiver that demodulates chip sequence by using zero-forcing equalization and hard-decision detection and detects the original bit sequence from the resulting detected chip sequence.

**B. Demodulation and Detection of DCSM**

At the receiver illustrated in Fig. 2, the received signal is passing through a normalized matched-filter $\tilde{g}_t(-t) = g_t(-t)/\sqrt{E_g}$ and sampled at $t = kT_c$, where $E_g = N_c P^2 T/3$ is the electrical energy of signal in (5). The sampled received signal can then be represented by

$$y_k = \sqrt{E_g} q_k * c_k + n_k,$$

(6)
Fig. 1. Example of DCSM scheme with reference OOK signal for bit sequence [0101101001]; (a) the proposed modulation scheme: DCSM with $N_c = 3$, (b) the proposed modulation scheme: DCSM with $N_c = 4$, (c) Chip-based signal representation equivalent to DCSM with $N_c = 3$, and (d) the reference scheme: OOK.

![Diagram of DCSM scheme](image)

Fig. 2. Block diagram of the equalized hard-decision DCSM receiver.

where

$$q_k = \begin{cases} 
1/4, & k = \pm 1 \\
1, & k = 0 \\
0, & \text{otherwise.}
\end{cases} \quad (7)$$

Each chip is inherently interfered by previous and next chip due to the signal generation of original bit sequence and this leads to the inter-chip interference (ICI) model in (6). In order to remove ICI, we utilize a zero-forcing equalizer (ZFE). The Z-transform in (6) is represented by $Y(z) = Q(z)C(z) + N(z)$, where we denote $Q(z) = 1 + 1/4z^{-1} + 1/4z$ for the Z-transform.

\(^2\)It is simple to implement and shown to provide the error rate performance comparable to the reference modulation schemes later.
of $q_k$ and $R_{nn}(z) = \frac{N_0}{2} Q(z)$ for the autocorrelation function of output noise.\textsuperscript{3} By applying the inverse of frequency response ICI channel, the ZFE is constructed as $F(z) = 1/Q(z)$. By taking the inverse Z-transform of $F(z)$, the infinite ZFE sequence can be computed as

$$f_k = \frac{2}{\sqrt{3}} \left( -2 + \sqrt{3} \right)^k u_k + \frac{2}{\sqrt{3}} \left( -2 - \sqrt{3} \right)^k u_{-k-1},$$

where $u_k$ is the discrete unit step function. We note that we utilize finite-length ZFE in which 21 taps in all integer $k \in [-10, 10]$ is enough to guarantee a negligible loss due to the finite length. It is obvious that this ZFE-based receiver is more complex to implement compared to the conventional modulation schemes. However, this ZFE utilizes the fixed weight which does not depend on the channel impulse response. Indeed, it does not require any weight update but only fixed number of multiplication and summation operations depending on the number of taps. Therefore, the computational complexity for decoding in the proposed scheme does not increase significantly. The equalizer output is given by $r_k = \sqrt{E_g c_k} + z_k$, where $z_k$ is the AWGN noise with zero mean and variance $\sigma_z^2 = \frac{N_0}{2} f_0$. Given the ZFE output $r_k$, the chip sequence is decoded

\textsuperscript{3}The Z-transform is defined as $X(z) = \sum_{k=-\infty}^{\infty} x_k z^{-k}$. 

---

![Flow chart of DCSM decoder in Fig. 2 and example for decoding the bit sequence [0101101001] when $N_c = 3$ in Fig. 1.](image)

Example: decoding of bit sequence for $N_c = 3$ in Fig 1

<table>
<thead>
<tr>
<th>$d_k$</th>
<th>$b_k$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>
based on maximum likelihood decision rule, i.e., the threshold detector decides the decoded output chips by the following hypothesis,

\[ r_k = \begin{cases} 1 & \text{if} \frac{E_g}{2} > \frac{\hat{c}_k}{c_k} \geq 0 \\ 0 & \text{otherwise} \end{cases} \]  

(9)

The decoded bit sequence is recovered from the decoded chip sequence via a DCSM decoder using the relation between bit and chip sequences. The flow chart for the DCSM decoder is illustrated in Fig. 3. It first recovers the input bit sequence with dummy bit 0. When the input bit 1 is sent, the \((N_c - 2)\) dummy bits 0 occurs before or after bit 1 since the chip duration of bit 1 is \((N_c - 1)\) times longer than a single chip. For oddly appeared bit 1, after the decoder checks if \((d_kd_{k+1} \cdots d_{k+N_c-2}) = (00 \cdots 01)\), \((N_c - 2)\) dummy bits 0 in front are removed, while \((N_c - 2)\) dummy bits 0 in back are removed after checking if \((d_kd_{k+1} \cdots d_{k+N_c-2}) = (100 \cdots 0)\) for evenly appeared bit 1.

III. PERFORMANCE ANALYSIS OF DCSM

A. Spectrum Analysis

In this section, we analyze the PSD of three schemes explained earlier. The transmit signal of input bit sequence is \(s(t) = \sum_{k=-\infty}^{\infty} x(t - kT)\). Note that the transmit signal is a cyclostationary random process which is a stochastic process with a periodic mean and autocorrelation function. First, we compute an autocorrelation function \(\phi_{ss}(t + \tau; t) = \mathbb{E}[s(t)s(t + \tau)]\) and average it over a single period \(T\) to eliminate the dependency on \(t\), i.e.,

\[ \tilde{\phi}_{ss}(\tau) = \frac{1}{T} \int_{-T/2}^{T/2} \phi_{ss}(t + \tau; t)dt. \]

(10)

Then, the Fourier transform of the autocorrelation function yields the PSD of \(s(t)\) as \(\Phi_{ss}(f) = \mathcal{F}[\tilde{\phi}_{ss}(\tau)]\). Substituting (4) into (10) and after some manipulation, the PSD of DCSM signals is computed as

\[ \Phi_{ss}(f) = \frac{1}{T_c} |G_t(f)|^2 \sum_{m=-\infty}^{\infty} \phi_{cc}(m)e^{-j2\pi fmT_c}, \]

(11)

where

\[ G_t(f) = \mathcal{F}[g_t(t)] = \frac{N_c}{2} P_T c \text{sinc}^2(fT_c) \]

(12)
and the correlation function of $c_k$ is given by

$$\phi_{cc}(m) = \mathbb{E}[c_k c_{k+m}] = \frac{1}{N_c} \sum_{n=0}^{\lfloor m/(N_c-1) \rfloor} \frac{|m-2n(N_c-2)| C_{2n}}{2|m-2n(N_c-2)|}. \quad (13)$$

The details of the derivation for $\phi_{cc}(m)$ are given in the Appendix. We note that $\phi_{cc}(m)$ converges to $\mathbb{E}[c_k]^2 = \frac{1}{N_c^2}$ as $m$ goes to infinity in accordance to the intuition that the farther two chips are away from each other, the less correlation they have. We approximate $\phi_{cc}(m) \approx \frac{1}{N_c^2}$ for $m > M$, where $M$ is a predetermined parameter set to 20 with reasonable accuracy in this paper. Then, we approximately find the closed form of PSD for DCSM;

$$\Phi_{ss}(f) \approx \frac{P^2 T}{2} \sin^4 \left( \frac{2 f T}{N_c} \right) \sum_{m=-M}^{M} \left( \sum_{n=0}^{\lfloor m/(N_c-1) \rfloor} \frac{|m-2n(N_c-2)| C_{2n}}{2|m-2n(N_c-2)|} - \frac{1}{N_c} \right) \times e^{-j \frac{4\pi f m T}{N_c}} + \frac{P^2}{4} \delta(t). \quad (14)$$

### B. Error Rate Analysis

We evaluate the error rate performance of DCSM using chip-based ZFE hard-decision threshold decoding. We first calculate the chip error rate performance. Given the ZFE output $r_k$, the received SNR for $c_k = 1$ is $\text{SNR}_d = \frac{E_g}{f_0 N_0}$. By computing the minimum distance over the binary signal set corresponding to $c_k$, the chip error probability for ZFE hard-decision DCSM receiver is given by

$$P_d = Q \left( \frac{\sqrt{E_g}}{2\sigma_z} \right) = Q \left( \sqrt{\frac{N_c P^2 T}{6 f_0 N_0}} \right). \quad (15)$$

Compared to the BER of the reference schemes, the loss due to above DCSM hard-decision receiver is almost $10 \log_{10}(\frac{N_c}{3 f_0})$ dB away from the bit error probability of OOK and PPM optimum receiver but it provides $10 \log_{10}(\frac{N_c}{f_0})$ dB SNR gain over the PDSM optimum receiver.

We note that a single-chip error in the DCSM scheme is propagated to the following bit sequence and affects the decoding of the following bit sequence. This makes the usual definition of bit error rate meaningless for our DCSM analysis. Therefore, we investigate packet error rate (PER) performance because an entire packet may be somewhat useless with any part in error and higher-layer design may desire knowledge of packet error to employ error control and automatic retransmission requests. Depending on the input bit sequence, i.e., distribution of total numbers
of bit 1 and 0 in a packet, the chip sequence has variable length since DCSM scheme sends the transmit signal with different duration according to binary bit. Assuming that a packet consist of \( L \) input bits, the PER of DCSM can be computed as

\[
\text{PER}_d = \sum_{l=0}^{L} p_1(l) \left(1 - (1 - P_d)^{L + (N_c-2)l}\right)
\]

\[
= 1 - \left(\frac{(1 + (1 - P_d)^{N_c-2})}{2}\right)^L,
\]

where \( p_1(l) = \frac{L!}{(L-l)!l!} \) denotes the probability of \( l \) number of bit 1 in a packet. It is approximated by using \( (1 - (1 - P_d)^{L + (N_c-2)l}) \approx (L + (N_c - 2)l)P_d \) as \( \text{PER}_d \approx \frac{N_cL}{2} P_d \).

C. Trade-off between Power and Spectral Efficiencies

The proposed DCSM can exploit the trade-off between power and spectral efficiencies by adjusting the number of chips for sending a bit. In a concept explained earlier, the basic DCSM requires \( N_c \) chips to send both bit 0 and bit 1, i.e., one chip for bit 0 and \( (N_c - 1) \) chips for bit 1 respectively. As in the mode of operation in Table I, only first or last chip among \( N_c - 1 \) chips is used to change the state of amplitude level by using a slope pulse. As \( N_c \) increases, the power efficiency can be improved since the transmit signal has peaky pulse shape. On the other hand, the chip duration \( \frac{2T}{N_c} \) is decreased and therefore the PSD of DCSM becomes wider over frequency.

IV. Numerical Results

In this section, we show the PSD and error rate performance of the proposed PDSM compared with the conventional modulation schemes. We first assume AWGN channel and the bit duration of 0.5\( \mu s \) unless otherwise noted.

Fig. 4 illustrates the comparison of PSDs for OOK, PPM, PDSM, and proposed DCSM using \( N_c = 3 \) and 4 for \( T = 0.5\mu s \). For the purpose of comparison, all PSD curves are normalized by the same value of power density to make DC component of OOK unity. The PSDs of the reference modulation schemes are obtained in the previous work [5]. Subfigure embedded into Fig. 4 illustrates the high density region of DCSM for \( N_c = 4 \). First, we see that the analytic results of PSD for the proposed DCSM coincide exactly with the simulation results. We observe that the DCSM signals for \( N_c = 3 \) and 4 has more concentrated power spectrum compared with
OOK, PPM, and PDSM. As the chip duration decreases, i.e., $N_c$ increases, the transmit power is still distributed in the low frequency range compared with PPM and PDSM. If low-pass or band-pass optical filter is employed, the proposed DCSM signal can be less distorted than OOK, PPM and PDSM signals.

In Fig. 5, we show the simulation and analytic results on PER performance for comparison among OOK, 2PPM, PDSM, and the proposed DCSM schemes with different number of chips in an AWGN channel. We first note that the approximate PER of DCSM scheme is well matched with simulation. The proposed DCSM with $N_c = 3$ is only 0.72 dB away from the best performance by OOK or PPM, while it can provide 4 dB SNR gain over conventional PDSM. We observe that the proposed DCSM schemes with $N_c$ more than 3 give better PER performance than the conventional OOK and 2PPM. As $N_c$ increases, it becomes more power-efficient, while requiring the wider modulation bandwidth. We note that, for different packet length, there is no remarkable change in PER for all the schemes but gradual degradation of PER with increasing length.

Finally, we present the PER performance of different modulation schemes in a band-limited channel in Fig. 6. We fix the size of a packet to $L = 1000$ bits and $SNR = 15$ dB and thus the lower bound (LB) of each modulation scheme in simulation approaches the PER performance
in an AWGN channel which was obtained theoretically in the previous section and confirmed in Fig 5. For a band-limited channel, we simply assume that the overall channel response is an exponentially decaying with an exponential decay constant \( \omega_c \), i.e., \( h(t) = e^{-\frac{\omega_c}{\sqrt{2}} t} \), where \( \omega_c \) is the 3-dB cutoff frequency. We here set \( f_c = 1 \) GHz. This model is widely used to characterize the LED response which behaves like a low pass response [6]. Therefore, OOK modulation scheme is more reliable over entire data rate of interest since its PSD is highly distributed in the low frequency region as shown in Fig. 4. The PPM modulation scheme requires much larger modulation bandwidth and thus less bandwidth-efficient that others. For \( N_c = 3 \), the proposed DCSM outperforms 2PPM in high data rate region. OOK modulation scheme still gives better PER performance than DCSM with \( N_c = 3 \). However, as \( N_c \) increases by 4, the proposed DCSM outperforms OOK modulation scheme in low and intermediate data rate region until 200 Mbits/s and provides better reliability that 2PPM throughout the whole rate region of interest. We note that OOK modulation scheme enjoys relatively better channel condition that other modulation schemes since the channel considered here is similar to low pass response. However, if the channel impulse response is close to band-pass response, the PER of OOK modulation might be degraded worse than the DCSM and 2PPM.

V. CONCLUSION

We developed a novel slope-based binary delay modulation called delayed chip slope modulation (DCSM) and its corresponding chip-based hard-decision receiver. Shorter chip durations than bit duration are used to exploit the trade-off between bandwidth and power efficiency. We analyzed the power spectral density and error rate performance of the proposed DCSM. We showed from numerical results that the DCSM scheme can exploit spectrum density more efficiently than the reference schemes while providing an error rate performance comparable to conventional modulation schemes.

APPENDIX

CORRELATION FUNCTION OF \( c_k \)

The correlation function of \( c_k \) is calculated by definition as

\[
\phi_{cc}(m) = \Pr[c_{k+m} = 1|c_k = 1] \Pr[c_k = 1],
\]
Theoretical Results for $L=1000$ bits

SNR ($\rho$) [dB]  

Packet Error Rate

PDSM
OOK & 2PPM
DCSM ($N_c=3$), sim
DCSM ($N_c=3$), approx
DCSM ($N_c=4$), sim
DCSM ($N_c=4$), approx
DCSM ($N_c=5$), sim
DCSM ($N_c=5$), approx

Fig. 5. Comparison of packet error rate for OOK, 2PPM, PDSM, and the proposed DCSM for different number of chips ($N_c$) with respect to $\text{SNR} = \frac{\rho}{2N_0}$ in an AWGN channel.

where $\Pr[c_k = 1] = \frac{1}{N_c}$ since $c_k = 1$ probably occurs once per $N_c$ chip durations by the mode of operation for DCSM. As we mentioned earlier, the sequence of $c_k$ is dependent on the information sequence of $b_i$. Given $c_k = 1$, $c_{k+m} = 1$ means that the state of amplitude level is the same. According to the mode of operation in DCSM scheme, a bit information of $b_i = 1$ changes the state of amplitude level. To remain the same state, bit information of $b_i = 1$ between $c_k$ and $c_{k+m}$ occurs evenly. Therefore, the above conditional probability is equivalent to the probability of all the cases that the number of bits of 1 between $c_k$ and $c_{k+m}$ is even. Let us assume $2n$ number of 1’s of $b_i$ between $c_k$ and $c_{k+m}$ for $n$ nonnegative integer. Then, total number of information bits between $c_k$ and $c_{k+m}$ is $m - 2n(N_c - 2)$, where $2n(N_c - 2)$ is the number of dummy bits occurred by $2n$ number of bit 1 between $c_k$ and $c_{k+m}$. The probability that the number of bits of 1 equals to $2n$ among $m - 2n(N_c - 2)$ bits is $\frac{m - 2n(N_c - 2)}{2m - 2n(N_c - 2)} C_{2n}$. Two information bits of 1 correspond to four bits of $c_k$ and, as such, the maximum possible number of information bit pairs of 1 between $c_k$

\footnote{For instance, see the bit and chip sequences in Fig. 1. There are four 1’s positioned on $\{b_4, b_5, b_6, b_8\}$ between $c_3$ and $c_{13}$.}

\footnote{The information bits are mutually independent.}
and $c_{k+m}$ is $\left\lfloor \frac{m}{2(N_c-1)} \right\rfloor$. Therefore, the above conditional probability can be calculated as

$$
\Pr \left[ c_{k+m} = 1 \middle| c_k = 1 \right] = \sum_{n=0}^{\left\lfloor \frac{m}{2(N_c-1)} \right\rfloor} \frac{m-2n(N_c-2)C_{2n}}{2m-2n(N_c-2)}. \tag{17}
$$

By the symmetry of correlation function $\phi_{cc}(m) = \phi_{cc}(-m)$, the correlation function of $c_k$ is finally given by

$$
\phi_{cc}(m) = \frac{1}{N_c} \sum_{n=0}^{\left\lfloor \frac{m}{2(N_c-1)} \right\rfloor} \frac{|m|-2n(N_c-2)C_{2n}}{2|m|-2n(N_c-2)}. \tag{18}
$$

REFERENCES


